Intel® Integrated Performance Primitives for Linux*

Agenda

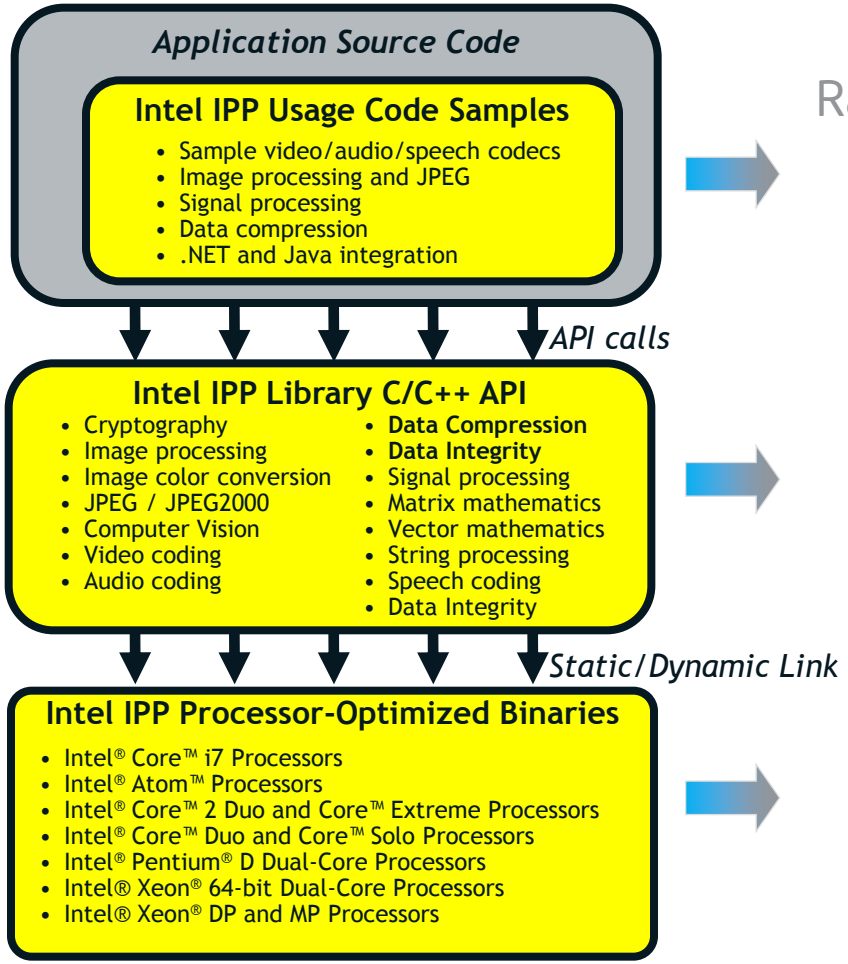
- System requirements, installation and environment
- Overview
- Main features & optimization(Code sample)
- Intel IPP function name convention
- Treading in Intel IPP
- Linkage model
- Intel® AVX Optimization

Intel IPP - overview

Free Code Samples

Cross-platform API

Processor-Optimized Implementation



Rapid Application Development

Compatibility and Code Re-Use

Outstanding Performance

Why are the functions fast?

- Intel® IPP functions exploit the instruction set architecture by
  - processing multiple data elements in parallel
    - Streaming SIMD Extensions like SSE4
  - processing data in larger chunks with each instruction
- Intel® IPP functions exploit the processor micro architecture by
  - pre-fetching data and avoiding cache blocking
  - resolving data and trace cache misses
  - avoiding branch mispredictions
- Intel® IPP functions use all execution resources available in the CPUs
  - Multi-Core Technology

Functions and Samples

Domains	Functions	Samples
1. Image Processing	* Geometry transformations, such as resize/rotate * Linear and non-linear filtering operation on an image for edge detection, blurring, noise removal and etc for filter effect. * Linear transforms for 2D FFTs, DFTs, DCT. * image statistics and analysis	* Tiled Image Processing / 2D Wavelet Transform /C++ Image Processing Classes/Image Processing functions Demo
2. Computer Vision	* Background differencing, Feature Detection (Corner Detection, Canny Edge detection), Distance Transforms, Image Gradients, Flood fill, Motion analysis and Object Tracking, Pyramids, Pattern recognition, Camera Calibration	* Face Detection
3. Color conversion	* Converting image/video color space formats: RGB, HSV, YUV, YCbCr * Up/Down sampling * Brightness and contrast adjustments	
4. JPEG Coding	* High-level JPEG and JPEG2000 compression and decompression functions * JPEG/JPEG2000 support functions: DCT, Wavelet transforms, color conversion, downsampling	• UIC-Unified Image Codec/ Integration with the Independent JPEG Group (IJG) library
5. Video Coding	* VC-1, H.264, MPEG-2, MPEG-4, H.261, H.263 and DV codec support functions	* Simple Media Player/ Video Encoder / h.264 decoding
6. Audio Coding	* Echo cancellation and audio transcoding, BlockFiltering, Spectral Data prequantization.	* Audio Codec Console application
7. Realistic Rendering	* Acceleration Structures, Ray-Scene Intersection and Ray Tracing * Surface properties, shader support, tone mapping	* Ray Tracing

Functions and Samples

Domains	Functions	Samples
8. Speech Coding	* Adaptive/Fixed Codebook functions, Autocorrelation, Convolution, Levinson-Durbin recursion, Linear Prediction Analysis & Quantization, Echo Cancellation, Companding	* G.168, G.167, G.711, G.722, G.722.1, G.722.2, AMRWB, Extended AMRWB (AMRWB+), G.723.1, G.726, G.728, G.729, RT-Audio, GSM AMR, GSM FR
9. Data Integrity	▪ Error-Correcting Codes ▪ Reed-Solomon	
10. Data Compression	* Entropy-coding compression: Huffman, VLC * Dictionary-based compression: LZSS, LZ77 * Burrows-Wheeler Transform, MoveToFront, RLE, Generalized Interval Transformation * Compatible feature support for zlib and bzip2	* zlib, bzip2, gzip-compatible /General data compression examples
11. Cryptography	* Big-Number Arithmetic / Rijndael, DES, TDES, SHA1, MD5, RSA, DSA, Montgomery, prime number generation and pseudo-random number generation (PRNG) functions	* Intel IPP crypto usage in Open SSL*
12. String Processing	* Compare, Insert, change case, Trim, Find, Regexp, Hash	* "ippgrep" – regular expression matching

Functions and Samples

Domains	Functions	Samples
13. Signal Processing	* Transforms: DCT, DFT, MDCT, Wavelet (both Haar and user-defined filter banks), Hilbert * Convolution, Cross-Correlation, Auto-Correlation, Conjugate * Filtering: IIR/FIR/Median filtering, Single/Multi-Rate FIR LMS filters * Other: Windowing, Jaehne/Tone/Traingle signal generation, Thresholding	* Signal Processing Function Demo
14. Vector Math	* Logical, Shift, Conversion, Power, Root, Exponential, Logarithmic, Trigonometric, Hyperbolic, Erf, Erfc	
15. Matrix Math	* Addition, Multiplication, Decomposition, Eigenvalues, Cross-product, transposition	
Other Common Functions	* CPUTypes, Thread Number Control, Memory Allocation	* Linkages/Different language support

Intel IPP is suitable for a very wide range of applications

Video broadcasting, Video/Voice Conferencing

Consumer Multimedia

Medical Imaging, Document Imaging

Computer Vision /Object Tracking / Machine Learning

Databases and Enterprise Data Management

Information Security

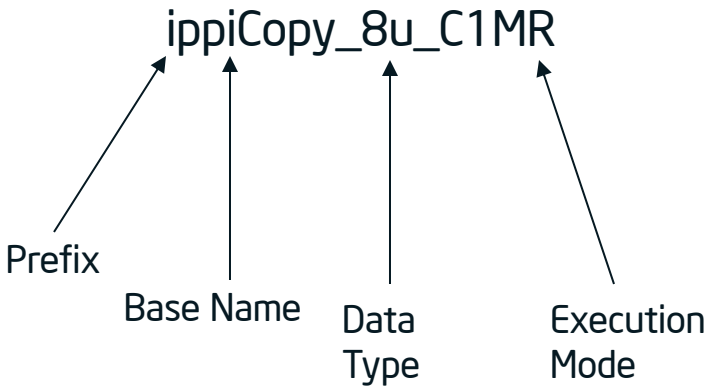
Embedded Applications

Mathematical and Scientific

Intel® IPP function naming convention and usage

Function names

- ✓ are easy to understand
- ✓ directly indicate the purpose of the function via distinct elements
- ✓ each element has a fixed number of pre-defined values



Name Elements	Description	Examples
Prefix	Indicates the functional data type in 1D , 2D and Matrix	ipps, ippi, ippm
Base Name	Abbreviation for the core operation	Add, FFTFwd, LuDecomp
Data Type	Describes bit depth and sign	8u, 32f, 64f
Execution mode	Indicates data layout and scaling	ISfs, C1R, P

Each function performs a particular operation on a known type of data in a specific mode

Intel® IPP libraries components

Header files, Dynamic and Static Libraries are sorted by Domains.

The dispatcher libraries and SSE-based optimized libraries are included in both Dynamic and Static Libraries

For example:

Domains	Header File	Dynamic Linking	Static Linking
Video Coding (vc)	*ippvc.h*	*ippvc.lib,* *ippvc.dll*	*lppvc_l.lib,* *lppvc_t.lib*

Function implementation

Intel IPP uses codes optimized for various central processing units (CPUs). Dispatching refers to detection of your CPU and selecting the corresponding Intel IPP binary. For example, ippiv8-7.0.dll in the \redist\ia32\ipp directory, reflects the imaging processing libraries optimized for the Intel(R) Core(TM) 2 Duo processors.

Platform	Identifier	Optimization
IA-32 Intel® Architecture	px	C-optimized for all IA-32 processors
	v8	Optimized for processors with Intel® Supplemental Streaming SIMD Extensions 3 (Intel SSSE3)
	p8	Optimized for processors with Intel® Streaming SIMD Extensions 4.1 (Intel SSE4.1)
	s8	Optimized for the Intel® Atom™ processor
Intel® 64 (Intel® EM64T) architecture	mx	C-optimized for processors with Intel® 64 instructions set architecture
	u8	Optimized for 64-bit applications on processors with Intel® Supplemental Streaming SIMD Extensions 3 (Intel SSE3)
	y8	Optimized for 64-bit applications on processors with Intel® Streaming SIMD Extensions 4.1 (Intel SSE4.1)
	n8	Optimized for the Intel® Atom™ processor
	e9	Optimized for processors that support Intel® Advanced Vector Extensions instruction set

Intel ® IPP gets updated with these libs to match the latest CPU features

Threading control flexibility in Intel® IPP

Intel® IPP are thread-safe. It supports threading above it:

- Intel® IPP threading functions are self-contained, which do not necessarily require application level threading to use OpenMP*
- Intel® IPP threading can be disabled or fine-tuned by applications

In a case that application needs fine-grained threading control

- Call the function *ippSetNumThreads* with argument 1
- Use static library to avoid OpenMP dependency
- Use completely single thread ideal for kernel development

Threading in Intel® IPP functions

Many computational intensive functions are threaded

Many (~2480) of Intel IPP functions are threaded.

- Where it improves performance

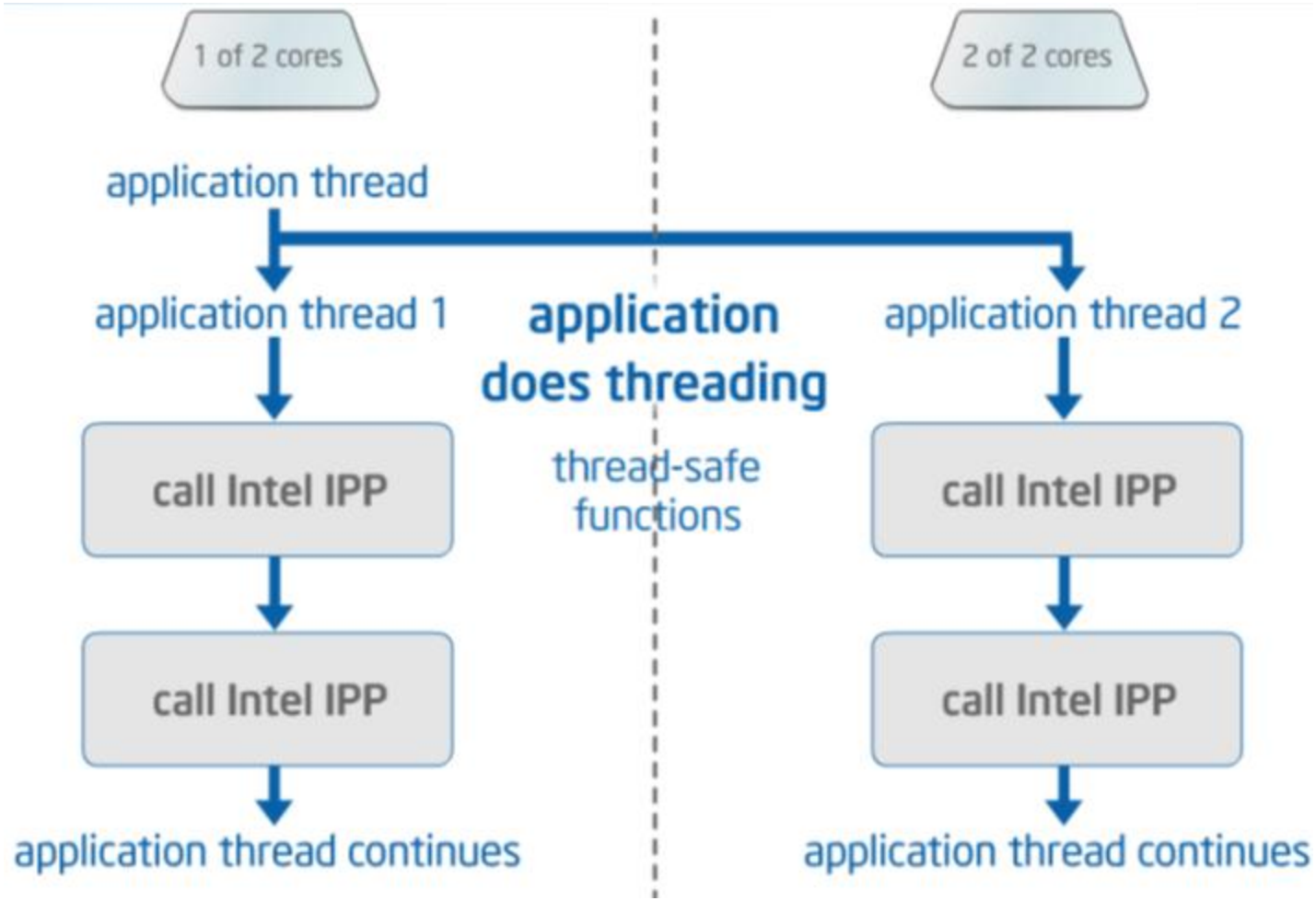
Usage model:

- Intel IPP threading Control
  - *ippSetNumThreads*
  - *ippGetNumThreads*

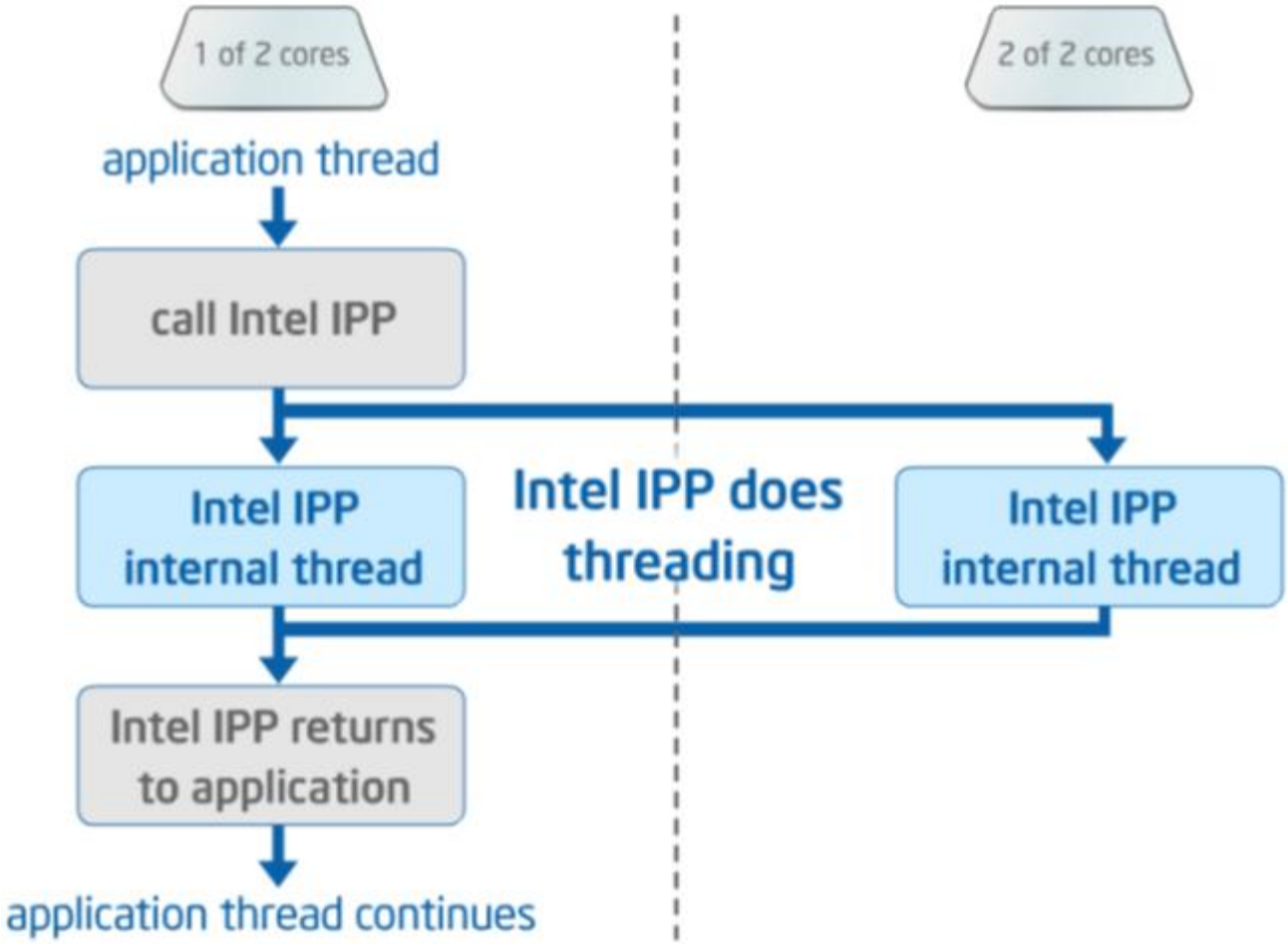
Domains	Threaded Functions
ippi	1346
ippr	11
ipm	527
ipps	586

Intel IPP functions are threaded when it maximizes performance

Threading in application



Threading inside Intel® IPP



Intel® IPP - linking options

- ✓ Dynamic linking using the run-time dynamic link libraries
- ✓ Static linking with dispatching by using emerged and merged static libraries
- ✓ Static linking without automatic dispatching using merged static libraries
- ✓ Dynamically building your own, custom, dynamic link library

What are the main differences?

- ✓ Code size(application executable or application installation package)
- ✓ Distribution method
- ✓ Processor coverage
- ✓ Application executes in kernel mode?

Dynamic linking

Dynamic linking is the simplest method and the most commonly used. It takes full advantage of

the dynamic dispatching mechanism in the dynamic link libraries (DLLs)

To dynamically link with Intel ® IPP, follow these steps:

1. Include **ipp.h** in your application. This header includes the header files for all Intel IPP functional domains.
2. Use the normal Intel IPP function names when calling the functions.
3. Link corresponding **domain import libraries**. For example, if you use the function ippsCopy_8u, link to ipps.lib.
4. Make sure that the run-time libraries are on the executable search path at run time. Run the ippvars.bat from directory **\ipp\bin** to ensure that the application loads the appropriate processor-specific library.

Static Linking with Dispatching

✓To use the static linking libraries, you need to link to all required domain libraries ipp*_l.lib, adding ippcore_l.lib and libraries on which domain libraries depend (see next section below). The * denotes the appropriate function domain.

✓If you want to use the Intel IPP functions threaded with the OpenMP*, you need to link to the threaded versions of the libraries ipp*_t.lib, ippcore_t.lib, and libiomp5md.lib.

All domain-specific and core libraries are located in the \ipp\lib\<arch> directory.

Static Linking without Dispatching

Benefits	Drawbacks
▪ Small executable size with support for only one processor type ▪ Suitable for kernel-mode/device-driver/ring-0 ▪ Suitable for a Web applet or a plug-in requiring very small file download and support for only one processor type ▪ Self-contained application executable that does not require the Intel IPP run-time DLLs ▪ Smallest footprint for application package ▪ Smallest installation package	•The executable is optimized for only one processor type • Updates to processor-specific optimizations require rebuild and/or relink

Custom Dynamic Linking

Benefits	•Drawbacks
▪ Run-time dispatching of processor-specific optimizations ▪ Reduced hard-drive footprint compared with a full set of Intel IPP DLLs ▪ Smallest installation package to accommodate use of some of the same Intel IPP functions by multiple applications	▪Application executable requires access to the Intel compiler specific run-time libraries that are delivered with Intel IPP ▪Developer resources are needed to create and maintain the custom DLLs ▪Integration of new processor-specific optimizations requires rebuilding the custom DLL ▪Not appropriate for kernel-mode/device-driver/ring-0 code

Intel® IPP Supported Linkage Model - quick comparison

Feature →	Dynamic Linkage	Static Linkage with Dispatching	Static Linkage without Dispatching	Using Custom DLL
Processor Updates	Automatic	Recompile & redistribute	Release new processor-specific application	Recompile & redistribute
Optimization	All processors	All processors	One processor	All processors
Build	Link to stub static libraries	Link to static libraries and static dispatchers	Link to merged libraries	Build separate DLL
Calling	Regular names	Regular names	Processor-specific names	Regular names
Distribution	Distribute linked IPP dll	No extra Distribution	No extra distribution	Distribute custom dll
Total Binary Size	Large	Small	Smallest	Small
Executable Size	Smallest	Small	Small	Smallest
Kernel Mode	No	Yes	Yes	No
Multi Threading Support	Yes	Yes, when linking with threaded static merged libraries	No	No

Intel® IPP provides a lot of flexibility

Intel® AVX Optimization

Intel® AVX (Intel® Advanced Vector Extensions) is a 256-bit instruction set extension to SSE designed to provide even higher performance for applications that are floating-point intensive.

Benefits of Intel AVX

✓Support for wider vector data (up to 256-bit).

✓Efficient instruction encoding scheme that supports 3 and 4 operand instruction syntaxes.

✓Flexible programming environment, ranging from branch handling to relaxed memory alignment requirements.

✓New data manipulation and arithmetic compute primitives, including broadcast, permute, fused-multiply-add, etc.

IPP Functions - Intel® AVX Optimization techniques

- Intel AVX optimization in the Intel IPP library consists of "hand-optimized" and "compiler tuned" function

- *ippGetCpuFeatures()* reports information regarding the SIMD features available to your processor. Alternatively, *ippGetCpuType()* detects the processor type in your system. A return value of *ippCpuAVX* means your processor supports the Intel AVX instruction set. These functions are declared in *ippcore.h*.

- Intel AVX SIMD instructions are supported by your processor, if *ippGetCpuFeatures()* return value *ippCPUID_AVX* (0x0100)

- Intel AVX SIMD instructions are supported by your operating system, mask the returned value from *ippGetCpuFeatures()* with *ippAVX_ENABLEDBYOS* (0x0200).

- Those functions that have not been directly optimized for AVX have been compiled using the Intel Compiler "xG" switch.

- For those functions that are not directly optimized for AVX, the g9/e9 library utilizes optimizations from prior compatible SSE optimizations, such as those tuned for the p8/y8 libraries and preceding SIMD optimizations (e.g., SSE4.x, AES-NI and SSE2/3).

List of functions optimized for Intel AVX

Mainly following domain APIs are directly optimized for Intel AVX

- Signal Processing
- Image Processing
- SPIRAL (GEN) Functions
- Audio Coding
- Speech Coding
- Color Conversion
- Realistic Rendering
- Computer Vision
- Image Compression

Detailed list of functions are in the Knowledge Base article,

http://software.intel.com/en-us/articles/intel-ipp-functions-optimized-for intel-avx-intel-advanced-vector-extensions/

Intel AVX Optimization : Speech Codec Performance Comparison(NHM Vs. SNB)

IA32

Intel® IPP SC Codec		Bitrate (bps)	Audio file		NHM (Nehalem)		SNB (Sandy Bridge)		Speedup : NHM/SNB	
	Voice Activity Detection			Duration (sec)	Encode (MHz)	Decode (MHz)	Encode (MHz)	Decode (MHz)	Encode	Decode
IPP_MSRTA_FP	-	8800	s_8000_16.wav	1070	20.42	2.35	16.65	1.92	1.23	1.22
IPP_MSRTA_FP	VAD1	8800	s_8000_16.wav	1070	19.97	2.15	16.45	1.78	1.21	1.21

Intel® IPP SC Codec		Bitrate (bps)	Audio file		NHM (Nehalem)		SNB (Sandy Bridge)		Speedup : NHM/SNB	
	Voice Activity Detection			Duration (sec)	Encode (MHz)	Decode (MHz)	Encode (MHz)	Decode (MHz)	Encode	Decode
IPP_MSRTA_FP	-	18000	s_16000_16.wav	1090	42.87	5.29	38.35	4.18	1.12	1.27
IPP_MSRTA_FP	VAD1	18000	s_16000_16.wav	1090	37.52	5.61	32.51	4.65	1.15	1.21

Intel64

Intel® IPP SC Codec	ippscy8-7.0.dll+	Bitrate (bps)	Audio file		NHM (Nehalem)		SNB (Sandy Bridge)		Speedup : NHM/SNB	
	Voice Activity Detection			Duration (sec)	Encode (MHz)	Decode (MHz)	Encode (MHz)	Decode (MHz)	Encode	Decode
IPP_MSRTA_FP	-	8800	s_8000_16.wav	1070	22.8	3.03	16.79	1.95	1.36	1.55
IPP_MSRTA_FP	VAD1	8800	s_8000_16.wav	1070	21.77	2.78	16.19	1.75	1.34	1.59

Intel® IPP SC Codec	ippscy8-7.0.dll+	Bitrate (bps)	Audio file		NHM (Nehalem)		SNB (Sandy Bridge)		Speedup : NHM/SNB	
	Voice Activity Detection			Duration (sec)	Encode (MHz)	Decode (MHz)	Encode (MHz)	Decode (MHz)	Encode	Decode
IPP_MSRTA_FP	-	18000	s_16000_16.wav	1090	46.26	6.87	34.51	4.36	1.34	1.58
IPP_MSRTA_FP	VAD1	18000	s_16000_16.wav	1090	39.99	7.25	31.08	4.77	1.29	1.52

Intel AVX Optimization : Performance data

Data compression functions performance data on SNB -
http://software.intel.com/en-us/articles/intel-ipp/#details

What's NEW in IPP 7.0

- New performance optimizations for the Intel® Advanced Vector Extensions (Intel AVX) for faster floating point operations in signal processing and image processing domains for the upcoming Sandy Bridge processors.

2/20/2013

- Intel® AES-NI optimization

  Advanced Encryption Standard New Instructions (AES-NI) introduced in the new generation of Intel® Core™ i7 Processor (Westmere microarchitecture) offer a significant increase in performance on cryptography and data compression.

- **Data Compression Library support (bzip2, zlib, gzip)**

✓ New Optimization in ipp_bzip2 to get better performance gain

✓ CRC32C (WSM new instruction) introduced into ipp_bzip2 to maximize performance

✓ New ipp_lzopack sample

✓ OpenMP optimization for ipp_zlib sample code

New IPP Features

- Improved JPEG codec multicore performance scaling, now up to 6x speedup on 8-core systems.

- JPEG-XR support in IPP

Supports lossless and lossy compression as well as incremental decompression of specific image regions

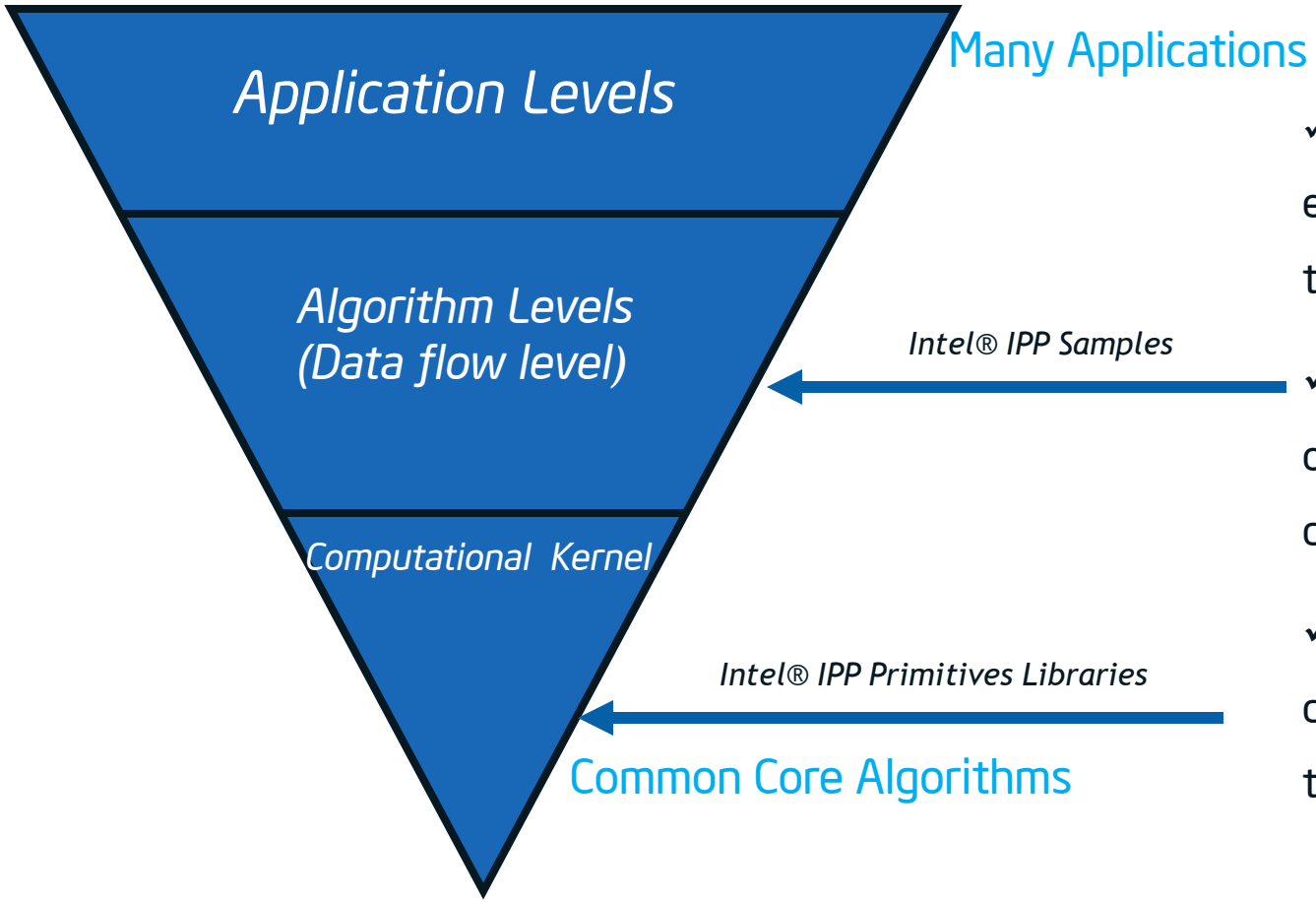
✓ Supports higher dynamic range and color depth than existing image codecs

✓ Intel IPP codec implementation features

- Unified Image Codec (UIC) JPEG-XR sample encoder and decoder with optional tile support for RGB color images with and without alpha channel and grayscale images with different bit depths.

- Intel IPP library support for JPEG-XR forward and inverse core transforms for 16s, 32s and 32f data types and Variable length code (VLC) encode and decode for 32s data types.

Conclusion



✓ Take Multiple Levels of efforts to optimized for threading

✓ Intel® IPP Libraries help you on primitives threading if your data allow

✓ Intel® IPP Samples demonstrate how you can thread at the algorithm levels

References

Intel® IPP Product Information

- http://www.intel.com/software/products/ipp

Technical Issues

- http://premier.intel.com/

- **Self-help**
  - http://www.intel.com/software/products/ipp
    (Click "Support Resource")

User Discussion Forum

- http://softwareforums.intel.com/ids/board?board.id=IPP

Book

- How to Optimize Applications Using Intel® IPP by Stewart Taylor
- http://www.intel.com/intelpress/sum_ipp.htm

Legal Disclaimer & Optimization Notice

INFORMATION IN THIS DOCUMENT IS PROVIDED "AS IS". NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO THIS INFORMATION INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Optimization Notice

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804