DEVELOPED BY YOU
IDF15 INTEL DEVELOPER FORUM
Developing Best-In-Class Security Principles with Open Source Firmware

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Senior Principal Engineer Intel Corporation

STTS003
Agenda

• Problem Statement
• Ingredients
• System Management Mode (SMM)
• Open Platforms
Agenda

• Problem Statement

• Ingredients

• System Management Mode (SMM)

• Open Platforms
Platform Threats

- BIOS Malware
- UEFI Rootkits
- Bootkits
- SMM Rootkits
- Device FW Malware
- ACPI Rootkits
- Option ROM Malware
- Evil Maid
- HVM Rootkits (Blue Pill)
- HW Trojans
Security Fundamentals
Security Fundamentals
What Could Possibly Go Wrong???

Power on ➔ [ .. Platform initialization . . ] ➔ [ .. OS boot . . . ] ➔ Shutdown

Security (SEC) Pre EFI Initialization (PEI) Driver Execution Environment (DXE) Boot Dev Select (BDS) Transient System Load (TSL) Run Time (RT) After Life (AL)
Agenda

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UEFI PI [Compliant] Firmware

CPU Reset

SEC

S-CRTM; Init caches/MTRRs; Cache-as-RAM (NEM); Recovery; TPM Init

Pre- EFI Init (PEI)

S-CRTM: Measure DXE/BDS
Early CPU/PCH Init
Memory (DIMMs, DRAM) Init

Driver Exec Env (DXE)

UEFI “Core” functionality, Continue initialization of platform & devices Enum FV, dispatch drivers (network, I/O, service..), Produce Boot and Runtime Services, SMM Initialization

Boot Dev Select (BDS)

Boot Manager (Select Boot Device)
EFI Shell/Apps; OS Boot Loader(s); Option ROM

Runtime / OS

ACPI, UEFI SystemTable, SMBIOS table,
Lock resources

ExitBootServices. Minimal UEFI services
(Variable, Capsule)
UDK2014 Available on Tianocore.org

**UDK2015 Coming Soon**

<table>
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<th>UDK2014 Releases</th>
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<td><strong>UDK2014.SP1.P1</strong></td>
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<td><strong>What is it?</strong></td>
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<td>UEFI development Kit 2014 SP1 Specification Release #1 (UDK2014.SP1.P1) (Complete zip of all packages and documentation where packages are expanded to MyWorkSpace Directory)</td>
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<td>Notes UDK2014.SP1</td>
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Usage of the EDK II Security Ingredients

System

Firmware

Protect

Detect

Recover
UEFI Secure Boot vs. TCG Trusted Boot

UEFI authenticate OS loader (pub key and policy)

Check signature of before loading

• UEFI Secure boot will stop platform boot if signature not valid (OEM to provide remediation capability)
• UEFI will require remediation mechanisms if boot fails

UEFI PI will measure OS loader & UEFI drivers into TPM (1.2 or 2.0) PCR (Platform Configuration Register)

• TCG Trusted boot will never fail
• Incumbent upon other software to make security decision using attestation
**RandomNumberGenerator**
- UEFI driver implementing the EFI_RNG_PROTOCOL from the UEFI2.4 specification

**Trusted Computing Group (TCG)**
- PEI Modules & DXE drivers implementing Trusted Computing Group measured boot
- EFI_TCG_PROTOCOL and EFI_TREE_PROTOCOL from the TCG and Microsoft® MSDN websites, respectively

**UserIdentification**
- DXE drivers that support multi-factor user authentication
- Chapter 31 of the UEFI 2.4 specification

**Library**
- DxeVerificationLib for “UEFI Secure Boot”, chapter 27.2 of the UEFI 2.4 specification + other support libs

**VariableAuthenticated**
- SMM and runtime DXE authenticated variable driver, chapter 7 of the UEFI2.4 specification

https://svn.code.sf.net/p/edk2/code/trunk/edk2/SecurityPkg
Additional Capabilities in Open Source

**Variable Lock Protocol**
Make variables read-only
[https://github.com/tianocore/edk2/blob/master/MdeModulePkg/Include/Protocol/VariableLock.h](https://github.com/tianocore/edk2/blob/master/MdeModulePkg/Include/Protocol/VariableLock.h)

**Lock Box**
Protect content across re-starts
[https://github.com/tianocore/edk2-MdeModulePkg/blob/master/Include/Protocol/LockBox.h](https://github.com/tianocore/edk2-MdeModulePkg/blob/master/Include/Protocol/LockBox.h)

**Capsule Update**
Generic capsule update driver support

**Recovery**
Device support for recovery from PEI
[https://svn.code.sf.net/p/edk2/code/trunk/edk2/MdeModulePkg/Include/Guid/RecoveryDevice.h](https://svn.code.sf.net/p/edk2/code/trunk/edk2/MdeModulePkg/Include/Guid/RecoveryDevice.h)

https://svn.code.sf.net/p/edk2/code/trunk/edk2/
/** Install child handles if the Handle supports GPT partition structure. 

Caution: This function may receive untrusted input.

The GPT partition table is external input, so this routine will do basic validation for GPT partition table before install child handle for each GPT partition.

@param[in] This       Calling context.
@param[in] Handle     Parent Handle.
@param[in] DevicePath Parent Device Path.

*/

EFI_STATUS PartitionInstallGptChildHandle

UEFI Development Kit 2010 example:
Full Verified Boot Sequence

CPU/SOC (Intel) -> Start Block PEI (OEM) -> BIOS DXE/UEFI (OEM) -> OS Loader/Kernel (OSV)

Intel® Boot Guard -> Executable -> Executable -> Executable

Policy Engine -> Policy -> Measure

Policy Engine -> Policy -> Measure

Policy Engine -> Policy -> Measure

Intel® Device Protection Technology with Boot Guard


OEM PI Verification Using PI Signed Firmware Volumes

Vol 3, section 3.2.1.1 of PI 1.3 Specification

OEM UEFI 2.4 Secure Boot

Chapter 27.2 of The UEFI 2.4 Specification

Intel® Device Protection Technology

Protect
Detect
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• Open Platforms
Full System Picture – UEFI PI Boot and Runtime

• Protect & Recover the UEFI PI implementation
  - UEFI Capsule Update
  - Hardware Secure Boot using Boot Guard on non-open platforms

• Detect if the Hypervisor and OS is expected one
  - UEFI Secure Boot (and TXT+LCP on non-open platforms)
  - EFI TCG Measured boot

• Protect at runtime
  - SMM Transfer Monitor (STM) to protect platform, hypervisor, and operating system (OS) from the BIOS SMM
BIOS Attack Surfaces

- Unsafe Coding Practices
- Shell Apps & Diags
- Option ROMs
- Standard APIs
- System Mgmt Mode
- BIOS Update Interfaces
- BIOS Vendor Hooks
- Server Mgmt Interfaces

UEFI, Open Platforms, and the Defender’s Dilemma

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CanSecWest 2015 Vancouver, Canada
System Management Mode (SMM)

- SMM is the most privileged software in the system
- It has access to all host accessible resources
  - Memory, TPM, chipset registers, device registers
  - It can be used to protect flash – *which contains UEFI code and variables*
- It is not affected by typical OS/VMM level software controls
  - Protection rings, paging, VMX...
  - System Management Interrupt (SMI) can’t be masked
  - SMRAM can’t be inspected & is transparent to typical system software
- It is commonly critical for proper system operation
- Mitigations
  - code review, validate internal/external input, no call outs
SystemManagement Mode RAM (SMRAM)

- Three SMRAM regions today: CSEG, HSEG (CSEG alias), and TSEG
  - CPU core's view of SMRAM based on internal register, SMBASE
    - SMM state save area
    - SMI entry point
- MSEG cleaved from top of TSEG on a 4K boundary
  - Related registers (programmed by BIOS):
    - IA32_SMM_MONITOR_CTL.MSEG_BASE
Orange regions are SMRAM
Software model defined in PI 1.4 specification, volume 4
Implementation at edk2\MdeModulePkg\Core\PiSmmCore
Intel® Virtualization Technology (Intel® VT)

VMEXIT Conditions
- CR0, CR4 accesses (basic CPU operations)
- CR3 writes (address space changes)
- CR3 reads, INVLP (paging)
- MSR & debug register accesses
- I/O instructions (per-port bitmap)
- CPUID, INVD
- Exceptions

VM Control Structure (VMCS)
- Which operations cause VMEXITs
- Which states change on VMEXITs and VMENTER
- VMM state area (state loaded on VMEXITs)
- Guest state area (saved on VMEXIT, restored on VMENTER)
SMI Transfer Monitor (STM)

- STM user guide defines software interfaces to manage:
  - Setup
  - Teardown
  - Steady state (runtime)
  - ... it also defines some optional ACPI and SMI based interfaces

- STM user guide does NOT define:
  - Protection policy
  - How protections are achieved
    - This is done using normal Intel® Architecture mechanisms (Intel VT, paging, etc.)

The STM provides isolation from the SMI handler
BIOS STM Opt-in

• BIOS should vigorously defend SMRAM
  - …because of its power, and critical importance to platform function
  - Therefore, BIOS must not enable an arbitrary or unknown STM

• BIOS populates MSEG with an STM image
  - BIOS should enforce it's own policy regarding what is an “acceptable” STM
    ▪ Likely policy:
      ❖ STM image supplied as part of BIOS flash image
      ❖ BIOS flash image has controlled updates (e.g. signed)
      ❖ Therefore: “I found it in my flash, so it’s acceptable”
    ▪ Many other BIOS policy options are possible

• IA32_SMM_MONITOR_CTL.[0] /* Valid bit */
  - BIOS sets to 1 if STM is present, BIOS clears to 0 (default) if no STM is present
  - Must be programmed identically across all CPU threads, Register only writable from SMM

• STM is idle and quiescent until it is “configured”
  - SMI is handled via legacy SMI mechanism
STM Image Format

### STM header
- Byte offset: 0
- Field: MSEG-header

### Dynamic STM code/data
- Byte offset: 2K
- Field: Static image size

### Static STM code/data
- Byte offset: 2K + 4
- Field: Per processor dynamic size

### STM header
- Byte offset: 2K + 8
- Field: Additional dynamic size

### STM features
- Byte offset: 2K + 12
- Field: STM features

### NumSmmRevIds
- Byte offset: 2K + 16

### SmmRevId[NumSmmRevIds]
- Byte offset: 2K + 20

---

### STM SMM revision ID

| Field   | 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Reserved|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| EM64T support | _1_ |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

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STM Features

STM SMM revision ID
Virtualization of BIOS SMI Handler

- SMI occurs - control is transferred to STM (VMEXIT)
- STM creates SMM state save area for BIOS
  - Scrubs register state if protected code has been interrupted by SMI
- STM resumes BIOS SMI handler in guest VM
- BIOS SMM code handles SMI
- STM traps on protected hardware accesses
  - Based on negotiated protection profile
- BIOS SMM executes RSM (VMEXIT) to STM
- STM restores interrupted VMs and resumes them
How to Declare Resources Allowed for SMM

- STM allocates hardware resources to BIOS SMI and MLE on a first-come-first-served basis. BIOS always has first opportunity to make a request
  - This is done statically via the BiosHwResourceRequirementsPtr
  - 64 bit physical pointer to a STMRESOURCE_LIST

```
<STMRESOURCE_LIST> ::= { <STM_RSC> } <STM_RSC_END>

<STM_RSC> ::= <STM_RSC_MEM_DESC>
|  <STM_RSC_IO_DESC>
|  <STM_RSC_PCI_CFG_DESC>
|  <STM_RSC_MSR_DESC>

<END> ::= <STM_RSC_END>
```
SMM Flow with STM

- firmware.intel.com to find STM user guide
- STM Reference implementation built on EDKII infrastructure
  - Build system, Mde Libraries, test driver and MinnowMax integration
Beyond STM Isolation, Moving to Testing

Usenix* WOOT 2015: KLEE → S2E →....

Symbolic execution for BIOS security

Oleksandr Bazhaniuk, John Loucaides, Lee Rosenbaum, Mark R. Tuttle, Vincent Zimmer

Intel Corporation

May 25, 2015

Abstract

We are building a tool that uses symbolic execution to search for BIOS security vulnerabilities including dangerous memory references (call outs) by SMM interrupt handlers in UEFI-compliant implementations of BIOS. Our tool currently applies only to interrupt handlers for SMM variables. Given a snapshot of SMRAM, the base address of SMRAM, and the address of the variable interrupt handler in SMRAM, the tool uses S2E to run the KLEE symbolic execution engine to search for concrete

This point exploded into public view [1] at the CanSecWest conference in March 2015. Among several interesting results was a paper provocatively titled “How many million BIOSes would you like to infect?” [2]. The authors made the following observation: Almost all machines are vulnerable because almost all machines are running unpatched BIOS (most consumers don’t know patches exist, and even sophisticated consumers apply patches with their fingers crossed), and widespread software reuse in the BIOS community (normally considered

WOOT 2015 Paper
chipsec

- A platform security assessment framework for risk assessment
- Can be extended to meet specific platform security concerns
- Open sourced https://github.com/chipsec/chipsec
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The Road from Core to Platform

Open Platforms & Reference Trees

- tianocore.org
- Open Source

OEM BIOS
- End users updating?
- Commercial product in the field
- Consumer product in the field

IBV
- ODMs updating?
- Existing ODM product

ODM BIOS
- New product

Time

KEY
- All
- Intel
- OEM
- IBV
- ODM
MinnowBoard Max

• Open hardware platform
• Intel® Atom™ SoC E38xx Series SoC single or dual core
• From http://firmware.intel.com/projects
• This project focuses in on the firmware source code (and binary modules) required to create the boot firmware image for the MinnowBoard MAX. The UEFI Open Source (EDKII project) packages for MinnowBoard MAX are available at http://tianocore.sourceforge.net/wiki/EDK2. To learn more about getting involved in the UEFI EDKII project visit the How to Contribute page.
• The source code builds using Microsoft Visual Studios* and GNU* C Compiler (for both 32 and 64 bit images) - production and debug execution environments. The source code builds the same UEFI firmware image shipping on MinnowBoard MAX.
• See more at: http://firmware.intel.com/projects#sthash.1oOc8srY.dpuf
MinnowBoard Max

• Focused on the maker community, but....

• 64-bit Intel® Atom™ SoC E38xx Series
• Has UEFI Secure Boot
• Built off of live tree
• Supports the SMM Transfer Monitor (STM) without Intel® Trusted Execution Technology (Intel® TXT)
• Ability to update with latest capabilities on http://www.tianocore.org
Intel® Quark™ SoC – Hardware Overview

- ISA-class 32 bit Intel® Pentium® processor
- PCI
- USB
- I2C
- Single core
UEFI for Intel® Quark™ SoC

• First fully open source Intel® Galileo based platform

• Builds on Intel® UDK2014 packages like MdePkg, MdeModulePkg w/ a 32-bit build, adding
  - IA32FamilyCpuBasePkg
  - QuarkPlatformPkg
  - QuarkSocPkg

• Standard build is 1 Mbyte image w/full features
  - Capsule update, SMM, S3, PCI, recovery, full UEFI OS support, FAT OS support, UEFI variables
Intel® Quark™ SoC and Security

- Support for I2C-attached TPM
- Hardware Secure Boot option
- UEFI Secure Boot implementation
- UEFI Capsule update support w/ hardware verification assist
- Demonstrates one way to build out UEFI Security Features with a full open source platform tree, with the following summary

| Platform          | Capsule update                        | UEFI Secure Boot | TCG Measured Boot | STM                  | chipsec
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<tr>
<td>MinnowBoard Max</td>
<td>Yes – with open source Capsule driver</td>
<td>Yes</td>
<td>Yes – Integrated TPM</td>
<td>Yes – VT w/o TXT</td>
<td>Yes</td>
</tr>
<tr>
<td>Intel® Quark™</td>
<td>Yes – with BootROM support</td>
<td>Yes</td>
<td>Yes – I2C TPM</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>Intel® Galileo</td>
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Summary and Next Steps

• Many security problems, including SMM escalation

• Open source ingredients

• New approach to handle SMM and Testing

• Use open platforms to demonstrate ingredients
Additional Sources of Information

- A PDF of this presentation is available from our Technical Session Catalog: www.intel.com/idfSessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.
- Booth info: #511

More information on security

- UEFI and PI specification – http://www.uefi.org
- EDK II Implementation – http://www.tianocore.org
- Platform Security information: https://firmware.intel.com/blog/
- EDK II Security Fixes: http://www.tianocore.org/security
- STM Specification and code: https://firmware.intel.com/content/smi-transfer-monitor-stm
- CHIPSEC: https://github.com/chipsec/chipsec/chipsec
- Intel® Quark™ Soc X1000 Version 1.1.0 BIOS https://downloadcenter.intel.com/download/23197/Intel-Quark-BSP
- MinnowMax http://www.minnowboard.org/meet-minnowboard-max/
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✓ = DONE
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You will receive an email with a link to the online evaluation prior to the end of this session.

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Intel® Compute Stick (20)

Day 2 Prize
Microsoft® Surface® 3 (6)

Day 3 Prize
Dell Venue 10 7000 Series (4)

Winners will be notified by email

Copies of the complete sweepstakes rules are available at the Info Desk
Q&A
WHAT WILL YOU DEVELOP?
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No computer system can be absolutely secure.

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