



# Intel Atom® Processor based on Tremont Microarchitecture

## Instruction Throughput and Latency

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**343370-001US**



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Date: May 2020 Tremont Microarchitecture Instruction Throughput and Latency

Instruction	Throughput	Latency	MSROM
ADC/SBB r32, imm8	1	2	N
ADC/SBB r64, imm8	1	2	N
ADC/SBB r32, r32	1	2	N
ADC/SBB r64, r64	1	2	N
ADD/AND/CMP/OR/SUB/XOR/TEST r32, r32	0.33	1	N
ADD/AND/CMP/OR/SUB/XOR/TEST r64, r64	0.33	1	N
ADDPD/ADDSUBPD/MAXPD/MINPD/SUBPD xmm, xmm	1	3	N
ADDPS/ADDSD/ADDSS/ADDSUBPS/SUBPS/SUBSD/SUBSS	1	3	N
MAXPS/MAXSD/MAXSS/MINPS/MINSD/MINSS xmm, xmm	1	3	N
ANDNPD/ANDNPS/ANDPD/ANDPS/ORPD/ORPS/XORPD/XORPS	0.5	1	N
AESDEC/AESDECLAST/AESEC/AESENCLAST	0.5	4	N
AESIMC/AESKEYGEN	0.5	4	N
BLENDDP/BLENDPS xmm, xmm, imm8	0.5	1	N
BLENDVPD/BLENDVPS xmm, xmm, <xmm0>	2	2	N
BSF/BSR r32, r32	1	3	N
BSF/BSR r64, r64	1	3	N
BSWAP r32	1	1	N
BSWAP r64	1	1	N
BT/BTC/BTR/BTS r32, r32	1	1	N
BT/BTC/BTR/BTS r64, r64	1	1	N
CBW/CWDE/CDQE	1	1	N
CWD	4	4	Y
CDQ/CQO/CLC/CMC	1	1	N
CMOVxx r32; r32	1	2	N
CMOVxx r64; r64	1	2	N
CMPPD xmm, xmm, imm	1	3	N
CMPSD/CMPPS/CMPSS xmm, xmm, imm	1	3	N
CMPXCHG r32, r32	5	5	Y
CMPXCHG r64, r64	5	5	Y
(U)COMISD/(U)COMISS xmm, xmm	1	5	N
CPUID	58	58	Y

CRC32 r32, r32	1	3	N
CRC32 r64, r64	1	3	N
CVTDQ2PD/CVTDQ2PS/CVTPD2DQ/CVTPD2PS xmm, xmm	1	4	N
CVT(T)PD2PI/CVT(T)PI2PD	1	4	N
CVT(T)PS2DQ/CVTPS2PD xmm, xmm;	1	4	N
CVT(T)SD2SS/CVTSS2SD xmm, xmm	1	4	N
CVTSI2SD/SS xmm, r32	1	7	N
CVTSD2SI/SS2SI r32, xmm	1	5	N
DEC/INC r32	1	1	N
DEC/INC r64	1	1	N
DIV r8 <sup>[3]</sup>	9-12	9-12	N
DIV r16 <sup>[3]</sup>	10-17	10-17	Y
DIV r32 <sup>[3]</sup>	10-25	10-25	Y
DIV r64 <sup>[3]</sup>	10-41	10-41	Y
DIVPD	16	21	N
DIVPS	10	15	N
DIVSD	8	13	N
DIVSS	5	10	N
DPPD xmm, xmm, imm	1	7	N
DPPS xmm, xmm, imm	1	10	N
EMMS	23	23	Y
EXTRACTPS	1	4	N
F2XM1	87	87	Y
FABS/FCHS	0.5	1	N
FCOM	1	3	N
FADD/FSUB	1	3	N
FCOS	154	154	Y
FDECSTP/FINCSTP	0.5	1	N
FDIV	5(SP)/8(DP)/9(EP)	10(SP)/13(DP)/14(EP)	N
FLDZ	1	4	N
FMUL	2	5	N
FPATAN/FYL2X/FYL2XP1	303	303	Y
FPTAN/FSINCOS	287	287	Y
FRNDINT	41	41	Y

FSCALE	32	32	Y
FSIN	140	140	Y
FSQRT	6(SP)/12(DP)/14(EP)	11(SP)/17(DP)/19(EP)	N
GF2P8AFFINEQB/GF2P8AFFINEINVQB	1	4	N
GF2P8MULB	1	4	N
HADDPD/HSUBPD xmm, xmm	5	5	Y
HADDPS/HSUBPS xmm, xmm	6	6	Y
IDIV r8 <sup>[3]</sup>	9-12	9-12	N
IDIV r16 <sup>[3]</sup>	9-17	9-17	Y
IDIV r32 <sup>[3]</sup>	9-25	9-25	Y
IDIV r64 <sup>[3]</sup>	9-41	9-41	Y
IMUL r32, r32 (single dest)	1	3	N
IMUL r32 (dual dest)	2	3 (4, EDX)	N
IMUL r64, r64 (single dest)	2	5	N
IMUL r64 (dual dest)	2	5 (6, RDX)	N
INSERTPS	0.5	1	N
MASKMOVDQU	4	4	Y
MOVAPD/MOVAPS/MOVDQA/MOVDQU/MOVUPD/MOVUPS xmm, xmm;	<a href="#">0.25<sup>[1]</sup>/0.5</a>	0/1	N
MOVD r32, xmm; MOVQ r64, xmm	1	5	N
MOVD xmm, r32 ; MOVQ xmm, r64	1	4	N
MOVDDUP/MOVHLPS/MOVLHPS/MOVSHDUP/MOVSLDUP	0.5	1	N
MOVDQ2Q/MOVQ/MOVQ2DQ	0.5	1	N
MOVSD/MOVSS xmm, xmm;	0.5	1	N
MPSADBW	1	4	N
MUL r32 (dual dest)	1	3 (4, EDX)	N
MUL r64 (dual dest)	1	5 (6, RDX)	N
MULPD; MULPS	1	4	N
MULSD; MULSS	1	4	N
NEG/NOT r32	0.33	1	N
NEG/NOT r64	0.33	1	N
PACKSSDW/WB xmm, xmm; PACKUSWB xmm, xmm	0.5	1	N
PABSB/D/W xmm, xmm	0.5	1	N
PADDD/D/W xmm, xmm; PSUBB/D/W xmm, xmm	0.5	1	N
PADDQ/PSUBQ/PCMPEQQ xmm, xmm	1	2	N

PADDSB/W; PADDUSB/W; PSUBSB/W; PSUBUSB/W	0.5	1	N
PALIGNR xmm, xmm	0.5	1	N
PAND/PANDN/POR/PXOR xmm, xmm	0.5	1	N
PAVGB/W xmm, xmm	0.5	1	N
PBLENDW xmm, xmm, imm	0.5	1	N
PBLENDVB xmm, xmm, <xmm0>	2	2	N
PCLMULQDQ xmm, xmm, imm	1	4	N
PCMPEQB/D/W xmm, xmm	0.5	1	N
PCMPESTR1 xmm, xmm, imm	8	$\frac{16^{(C)}}{17^{(F)[2]}}$	Y
PCMPESTRM xmm, xmm, imm	8	$\frac{11^{(X)}}{16^{(F)[2]}}$	Y
PCMPGTB/D/W xmm, xmm	0.5	1	N
PCMPGTQ/PHMINPOSUW xmm, xmm	2	5	N
PCMPISTR1 xmm, xmm, imm	8	$\frac{11^{(C)}}{12^{(F)[2]}}$	Y
PCMPISTRM xmm, xmm, imm	8	$\frac{6^{(X)}}{11^{(F)[2]}}$	Y
PEXTRB/WD r32, xmm, imm	1	5	N
PINSRB/WD xmm, r32, imm	1	5	N
PHADDD/PHSUBD xmm, xmm	4	4	Y
PHADDW/PHADDSW xmm, xmm	6	6	Y
PHSUBW/PHSUBSW xmm, xmm	6	6	Y
PMADDUBSW/PMADDWD/PMULHRW/PSADBW xmm, xmm	1	4	N
PMAXSB/W/D xmm, xmm; PMAXUB/W/D xmm, xmm	0.5	1	N
PMINSB/W/D xmm, xmm; PMINUB/W/D xmm, xmm	0.5	1	N
PMOVMASKB r32, xmm	1	5	N
PMOVSXBW/BD/BQ/WD/WQ/DQ xmm, xmm	0.5	1	N
PMOVZXBW/BD/BQ/WD/WQ/DQ xmm, xmm	0.5	1	N
PMULDQ/PMULUDQ xmm, xmm	1	4	N
PMULHUW/PMULHW/PMULLW xmm, xmm	1	4	N
PMULLD xmm, xmm	2	5	N
POPCNT r32, r32	1	3	N
POPCNT r64, r64	1	3	N
PSHUFB xmm, xmm	1	1	N
PSHUFD xmm, mem, imm	0.5	1	N
PSHUFBW; PSHUFLW; PSHUFW	0.5	1	N
PSIGNB/D/W xmm, xmm	0.5	1	N

PSLLDQ/PSRLDQ xmm, imm; SHUFPD/SHUFPS	0.5	1	N
PSLLD/Q/W xmm, xmm	1	2	N
PSRAD/W xmm, imm;	0.5	1	N
PSRAD/W xmm, xmm;	1	2	N
PSRLD/Q/W xmm, imm;	0.5	1	N
PSRLD/Q/W xmm, xmm	1	2	N
PTEST xmm, xmm	1	4	N
PUNPCKHBW/DQ/WD; PUNPCKLBW/DQ/WD	0.5	1	N
PUNPCKHQDQ; PUNPCKLQDQ	0.5	1	N
RCPPS/RSQRTPS	2	5	N
RCPSS/RSQRTSS	1	4	N
RDTSC	20	20	Y
ROUNDPD/PS	1	4	N
ROUNDSD/SS	1	4	N
ROL; ROR; SAL; SAR; SHL; SHR (count in CL)	1	1 (2 for CL source)	N
ROL; ROR; SAL; SAR; SHL; SHR (count in imm8)	1	1	N
SHA1MSG1/SHA1MSG2/SHA1NEXTE	1	3	N
SHA1RND4 xmm, xmm, imm	1	4	N
SHA256MSG1/SHA256MSG2	1	3	N
SHA256RND4	2	4	N
SAHF	1	1	N
SHLD r32, r32, imm	2	2	N
SHRD r32, r32, imm	2	2	N
SHLD/SHRD r64, r64, imm	12	12	Y
SHLD/SHRD r64, r64, CL	14	14	Y
SHLD/SHRD r32, r32, CL	4	4	Y
SHUFPD/SHUFPS xmm, xmm, imm	0.5	1	N
SQRTPD	24	29	N
SQRTPS	12	17	N
SQRTPD	12	17	N
SQRTPS	6	11	N
TEST r32, r32	0.33	1	N
TEST r64, r64	0.33	1	N
UNPCKHPD; UNPCKHPS; UNPCKLPD, UNPCKLPS	0.5	1	N



XADD r32, r32	4	4	Y
XCHG r32, r32	4	4	Y
XCHG r64, r64	4	4	Y

NOTES:

[\[1\]Throughput is 0.25 cycles if move elimination is in effect, otherwise 0.5 cycle.](#)

[\[2\]Latency values are for ECX/EFLAGS/XMM0 dependency: \(C/F/X\).](#)

[3] Variable latency instruction. Latency varies depending on source operand data value.