Intel® Xeon® Scalable Processor

Instruction Throughput and Latency

August 2017

Revision 1.1

336289-002

Revision History

Document ID	Description	Date
336289-001	Initial Release	Jul-17
336289-002	256bit memory accesses previously listed as having 0 cycles latency. Updated to 7 cycles.	Aug-17

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XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_ZMMu8_MEMu8_IMM8_AVX512	vpcmpub k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_IMM8_AVX512	vpcmpub k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_XMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_XMMu32_XMMu32_IMM8_AVX512	vpcmpud k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, ymm1, [rdi], 1	10	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vpcmpud k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vpcmpud k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_XMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_XMMu64_XMMu64_IMM8_AVX512	vpcmpuq k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, ymm1, [rdi], 1	10	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vpcmpuq k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vpcmpuq k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_XMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_XMMu16_XMMu16_IMM8_AVX512	vpcmpuw k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_YMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, ymm1, [rdi], 1	10	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_YMMu16_YMMu16_IMM8_AVX512	vpcmpuw k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_ZMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_IMM8_AVX512	vpcmpuw k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_XMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_XMMi16_XMMi16_IMM8_AVX512	vpcmpw k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_YMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, ymm1, [rdi], 1	10	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_YMMi16_YMMi16_IMM8_AVX512	vpcmpw k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_ZMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_ZMMi16_ZMMi16_IMM8_AVX512	vpcmpw k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_XMMu32_AVX512	vpcompressd [rdi]{k1}, xmm1	11	2
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_YMMu32_AVX512	vpcompressd [rdi]{k1}, ymm1	11	2
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_ZMMu32_AVX512	vpcompressd [rdi]{k1}, zmm1	11	2
XED_IFORM_VPCOMPRESSD_XMMu32_MASKmskw_XMMu32_AVX512	vpcompressd xmm1{k1}, xmm2	6	2
XED_IFORM_VPCOMPRESSD_YMMu32_MASKmskw_YMMu32_AVX512	vpcompressd ymm1{k1}, ymm2	6	2
XED_IFORM_VPCOMPRESSD_ZMMu32_MASKmskw_ZMMu32_AVX512	vpcompressd zmm1{k1}, zmm2	6	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_XMMu64_AVX512	vpcompressq [rdi]{k1}, xmm1	11	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_YMMu64_AVX512	vpcompressq [rdi]{k1}, ymm1	11	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_ZMMu64_AVX512	vpcompressq [rdi]{k1}, zmm1	11	2
XED_IFORM_VPCOMPRESSQ_XMMu64_MASKmskw_XMMu64_AVX512	vpcompressq xmm1{k1}, xmm2	6	2
XED_IFORM_VPCOMPRESSQ_YMMu64_MASKmskw_YMMu64_AVX512	vpcompressq ymm1{k1}, ymm2	6	2
XED_IFORM_VPCOMPRESSQ_ZMMu64_MASKmskw_ZMMu64_AVX512	vpcompressq zmm1{k1}, zmm2	6	2
XED_IFORM_VPCONFLICTD_XMMu32_MASKmskw_MEMu32_AVX512	vpconflictd xmm1{k1}, [rdi]	15	2.31
XED_IFORM_VPCONFLICTD_XMMu32_MASKmskw_XMMu32_AVX512	vpconflictd xmm1{k1}, xmm2	22	5
XED_IFORM_VPCONFLICTD_YMMu32_MASKmskw_MEMu32_AVX512	vpconflictd ymm1{k1}, [rdi]	44	9

XED_IFORM_VPCONFLICTD_YMMu32_MASKmskw_YMMu32_AVX512	vpconflictd ymm1{k1}, ymm2	37	9
XED_IFORM_VPCONFLICTD_ZMMu32_MASKmskw_MEMu32_AVX512CD	vpconflictd zmm1{k1}, [rdi]	74	17.5
XED_IFORM_VPCONFLICTD_ZMMu32_MASKmskw_ZMMu32_AVX512CD	vpconflictd zmm1{k1}, zmm2	67	17.5
XED_IFORM_VPCONFLICTQ_XMMu64_MASKmskw_MEMu64_AVX512	vpconflictq xmm1{k1}, [rdi]	11	2
XED_IFORM_VPCONFLICTQ_XMMu64_MASKmskw_XMMu64_AVX512	vpconflictq xmm1{k1}, xmm2	5	2
XED_IFORM_VPCONFLICTQ_YMMu64_MASKmskw_MEMu64_AVX512	vpconflictq ymm1{k1}, [rdi]	29	5
XED_IFORM_VPCONFLICTQ_YMMu64_MASKmskw_YMMu64_AVX512	vpconflictq ymm1{k1}, ymm2	22	5
XED_IFORM_VPCONFLICTQ_ZMMu64_MASKmskw_MEMu64_AVX512CD	vpconflictq zmm1{k1}, [rdi]	44	10.5
XED_IFORM_VPCONFLICTQ_ZMMu64_MASKmskw_ZMMu64_AVX512CD	vpconflictq zmm1{k1}, zmm2	37	10.5
XED_IFORM_VPERM2F128_YMMqq_YMMqq_MEMqq_IMMb	vperm2f128 ymm1, ymm2, [rdi], 1	10	1
XED_IFORM_VPERM2F128_YMMqq_YMMqq_YMMqq_IMMb	vperm2f128 ymm1, ymm2, ymm3, 1	3	1
XED_IFORM_VPERM2I128_YMMqq_YMMqq_MEMqq_IMMb	vperm2i128 ymm1, ymm2, [rdi], 1	10	1
XED_IFORM_VPERM2I128_YMMqq_YMMqq_YMMqq_IMMb	vperm2i128 ymm1, ymm2, ymm3, 1	3	1
XED_IFORM_VPERMD_YMMqq_YMMqq_MEMqq	vpermd ymm1, ymm2, [rdi]	10	1
XED_IFORM_VPERMD_YMMqq_YMMqq_YMMqq	vpermd ymm1, ymm2, ymm3	3	1
XED_IFORM_VPERMD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermd ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2D_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpermi2d xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2D_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpermi2d xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2D_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermi2d ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMI2D_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermi2d ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2D_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermi2d zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2D_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermi2d zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermi2pd xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermi2pd xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermi2pd ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMI2PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermi2pd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermi2pd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermi2pd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermi2ps xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermi2ps xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermi2ps ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMI2PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermi2ps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermi2ps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermi2ps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2Q_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpermi2q xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2Q_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpermi2q xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2Q_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermi2q ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMI2Q_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermi2q ymm1{k1}, ymm2, ymm3	3	1

XED_IFORM_VPERMI2Q_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermi2q zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2Q_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermi2q zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2W_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermi2w xmm1{k1}, xmm2, [rdi]	13	2
XED_IFORM_VPERMI2W_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermi2w xmm1{k1}, xmm2, xmm3	7	2
XED_IFORM_VPERMI2W_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermi2w ymm1{k1}, ymm2, [rdi]	14	2
XED_IFORM_VPERMI2W_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermi2w ymm1{k1}, ymm2, ymm3	7	2
XED_IFORM_VPERMI2W_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermi2w zmm1{k1}, zmm2, [rdi]	14	2
XED_IFORM_VPERMI2W_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermi2w zmm1{k1}, zmm2, zmm3	7	2
XED_IFORM_VPERMILPD_XMMdq_MEMdq_IMMb	vpermilpd xmm1, [rdi], 1	7	1
XED_IFORM_VPERMILPD_XMMdq_XMMdq_MEMdq	vpermilpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPD_XMMdq_XMMdq_IMMb	vpermilpd xmm1, xmm2, 1	1	1
XED_IFORM_VPERMILPD_XMMdq_XMMdq_XMMdq	vpermilpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermilpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vpermilpd xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermilpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPERMILPD_YMMqq_MEMqq_IMMb	vpermilpd ymm1, [rdi], 1	8	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_MEMqq	vpermilpd ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_IMMb	vpermilpd ymm1, ymm2, 1	1	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_YMMqq	vpermilpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermilpd ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vpermilpd ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermilpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermilpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vpermilpd zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermilpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPERMILPS_XMMdq_MEMdq_IMMb	vpermilps xmm1, [rdi], 1	7	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_MEMdq	vpermilps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_IMMb	vpermilps xmm1, xmm2, 1	1	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_XMMdq	vpermilps xmm1, xmm2, xmm3	1	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermilps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vpermilps xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermilps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPERMILPS_YMMqq_MEMqq_IMMb	vpermilps ymm1, [rdi], 1	8	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_MEMqq	vpermilps ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_IMMb	vpermilps ymm1, ymm2, 1	1	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_YMMqq	vpermilps ymm1, ymm2, ymm3	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps ymm1{k1}, [rdi], 1	8	1

XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermilps ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vpermilps ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermilps ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermilps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vpermilps zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermilps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPERMPD_YMMqq_MEMqq_IMMb	vpermpd ymm1, [rdi], 1	10	1
XED_IFORM_VPERMPD_YMMqq_YMMqq_IMMb	vpermpd ymm1, ymm2, 1	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermpd ymm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermpd ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vpermpd ymm1{k1}, ymm2, 1	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermpd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermpd zmm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermpd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vpermpd zmm1{k1}, zmm2, 1	3	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermpd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMPS_YMMqq_YMMqq_MEMqq	vpermps ymm1, ymm2, [rdi]	10	1
XED_IFORM_VPERMPS_YMMqq_YMMqq_YMMqq	vpermps ymm1, ymm2, ymm3	3	1
XED_IFORM_VPERMPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermps ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMQ_YMMqq_MEMqq_IMMb	vpermq ymm1, [rdi], 1	10	1
XED_IFORM_VPERMQ_YMMqq_YMMqq_IMMb	vpermq ymm1, ymm2, 1	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpermq ymm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermq ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpermq ymm1{k1}, ymm2, 1	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpermq zmm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpermq zmm1{k1}, zmm2, 1	3	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2D_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpermt2d xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2D_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpermt2d xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2D_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermt2d ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMT2D_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermt2d ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2D_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermt2d zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2D_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermt2d zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermt2pd xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermt2pd xmm1{k1}, xmm2, xmm3	3	1

XED_IFORM_VPERMT2PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermt2pd ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMT2PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermt2pd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermt2pd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermt2pd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermt2ps xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermt2ps xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermt2ps ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMT2PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermt2ps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermt2ps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermt2ps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2Q_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpermt2q xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2Q_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpermt2q xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2Q_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermt2q ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPERMT2Q_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermt2q ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2Q_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermt2q zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2Q_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermt2q zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2W_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermt2w xmm1{k1}, xmm2, [rdi]	13	2
XED_IFORM_VPERMT2W_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermt2w xmm1{k1}, xmm2, xmm3	7	2
XED_IFORM_VPERMT2W_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermt2w ymm1{k1}, ymm2, [rdi]	14	2
XED_IFORM_VPERMT2W_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermt2w ymm1{k1}, ymm2, ymm3	7	2
XED_IFORM_VPERMT2W_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermt2w zmm1{k1}, zmm2, [rdi]	14	2
XED_IFORM_VPERMT2W_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermt2w zmm1{k1}, zmm2, zmm3	7	2
XED_IFORM_VPERMW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermw xmm1{k1}, xmm2, [rdi]	12	2
XED_IFORM_VPERMW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermw xmm1{k1}, xmm2, xmm3	6	2
XED_IFORM_VPERMW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermw ymm1{k1}, ymm2, [rdi]	13	2
XED_IFORM_VPERMW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermw ymm1{k1}, ymm2, ymm3	6	2
XED_IFORM_VPERMW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermw zmm1{k1}, zmm2, [rdi]	13	2
XED_IFORM_VPERMW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermw zmm1{k1}, zmm2, zmm3	6	2
XED_IFORM_VPEXPANDD_XMMu32_MASKmskw_MEMu32_AVX512	vpexpandd xmm1{k1}, [rdi]	10	2
XED_IFORM_VPEXPANDD_XMMu32_MASKmskw_XMMu32_AVX512	vpexpandd xmm1{k1}, xmm2	4	2
XED_IFORM_VPEXPANDD_YMMu32_MASKmskw_MEMu32_AVX512	vpexpandd ymm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDD_YMMu32_MASKmskw_YMMu32_AVX512	vpexpandd ymm1{k1}, ymm2	4	2
XED_IFORM_VPEXPANDD_ZMMu32_MASKmskw_MEMu32_AVX512	vpexpandd zmm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDD_ZMMu32_MASKmskw_ZMMu32_AVX512	vpexpandd zmm1{k1}, zmm2	4	2
XED_IFORM_VPEXPANDQ_XMMu64_MASKmskw_MEMu64_AVX512	vpexpandq xmm1{k1}, [rdi]	10	2
XED_IFORM_VPEXPANDQ_XMMu64_MASKmskw_XMMu64_AVX512	vpexpandq xmm1{k1}, xmm2	4	2
XED_IFORM_VPEXPANDQ_YMMu64_MASKmskw_MEMu64_AVX512	vpexpandq ymm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDQ_YMMu64_MASKmskw_YMMu64_AVX512	vpexpandq ymm1{k1}, ymm2	4	2
XED_IFORM_VPEXPANDQ_ZMMu64_MASKmskw_MEMu64_AVX512	vpexpandq zmm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDQ_ZMMu64_MASKmskw_ZMMu64_AVX512	vpexpandq zmm1{k1}, zmm2	4	2
XED_IFORM_VPEXTRB_MEMb_XMMdq_IMMb	vpextrb [rdi], xmm1, 1	6	1

XED_IFORM_PEXTRB_MEMb_XMMdq_IMMb	vpextrb [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRB_MEMu8_XMMu8_IMM8_AVX512	vpextrb [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRB_GPR32u8_XMMu8_IMM8_AVX512	vpextrb eax, xmm1, 1	3	1
XED_IFORM_VPEXTRB_GPR32d_XMMdq_IMMb	vpextrb eax, xmm1, 1	3	1
XED_IFORM_PEXTRB_GPR32d_XMMdq_IMMb	vpextrb eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_MEMu32_XMMu32_IMM8_AVX512	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRD_MEMd_XMMdq_IMMb	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRD_MEMd_XMMdq_IMMb	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRD_GPR32d_XMMdq_IMMb	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_GPR32d_XMMdq_IMMb	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_GPR32u32_XMMu32_IMM8_AVX512	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRQ_MEMu64_XMMu64_IMM8_AVX512	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRQ_MEMq_XMMdq_IMMb	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRQ_MEMq_XMMdq_IMMb	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRQ_GPR64q_XMMdq_IMMb	vpextrq rax, xmm1, 1	3	1
XED_IFORM_PEXTRQ_GPR64q_XMMdq_IMMb	vpextrq rax, xmm1, 1	3	1
XED_IFORM_VPEXTRQ_GPR64u64_XMMu64_IMM8_AVX512	vpextrq rax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_MEMw_XMMdq_IMMb	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRW_SSE4_MEMw_XMMdq_IMMb	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRW_MEMu16_XMMu16_IMM8_AVX512	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRW_GPR32d_XMMdq_IMMb_C5	vpextrw eax, xmm1, 1	3	1
XED_IFORM_PEXTRW_GPR32_XMMdq_IMMb	vpextrw eax, xmm1, 1	3	1
XED_IFORM_PEXTRW_SSE4_GPR32_XMMdq_IMMb	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_GPR32d_XMMdq_IMMb_15	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_GPR32u16_XMMu16_IMM8_AVX512	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPGATHERDD_YMMu32_MEMqq_YMMi32_VL256	vpgatherdd ymm1, [rdi+ymm2*1], ymm	27	5
XED_IFORM_VPGATHERDD_YMMu32_MASKmskw_MEMu32_AVX512_VL256	vpgatherdd ymm1{k1}, [rdi+ymm2*1]	27	5
XED_IFORM_VPGATHERDD_ZMMu32_MASKmskw_MEMu32_AVX512_VL512	vpgatherdd zmm1{k1}, [rdi+zmm2*1]	30	9.75
XED_IFORM_VPGATHERDQ_XMMu64_MEMdq_XMMi64_VL128	vpgatherdq xmm1, [rdi+xmm2*1], xmm	22	2
XED_IFORM_VPGATHERDQ_XMMu64_MASKmskw_MEMu64_AVX512_VL128	vpgatherdq xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VPGATHERDQ_YMMu64_MEMqq_YMMi64_VL256	vpgatherdq ymm1, [rdi+xmm2*1], ymm	25	4
XED_IFORM_VPGATHERDQ_YMMu64_MASKmskw_MEMu64_AVX512_VL256	vpgatherdq ymm1{k1}, [rdi+xmm2*1]	25	4
XED_IFORM_VPGATHERDQ_ZMMu64_MASKmskw_MEMu64_AVX512_VL512	vpgatherdq zmm1{k1}, [rdi+ymm2*1]	26	5
XED_IFORM_VPGATHERQD_XMMu32_MEMq_XMMi32_VL128	vpgatherqd xmm1, [rdi+ymm2*1], xmm	20	2
XED_IFORM_VPGATHERQD_XMMu32_MEMdq_XMMi32_VL256	vpgatherqd xmm1, [rdi+ymm2*1], xmm	20	2
XED_IFORM_VPGATHERQD_XMMu32_MASKmskw_MEMu32_AVX512_VL256	vpgatherqd xmm1{k1}, [rdi+ymm2*1]	20	2
XED_IFORM_VPGATHERQD_XMMu32_MASKmskw_MEMu32_AVX512_VL128	vpgatherqd xmm1{k1}, [rdi+ymm2*1]	20	2
XED_IFORM_VPGATHERQD_YMMu32_MASKmskw_MEMu32_AVX512_VL512	vpgatherqd ymm1{k1}, [rdi+zmm2*1]	25	4
XED_IFORM_VPGATHERQQ_XMMu64_MEMdq_XMMi64_VL128	vpgatherqq xmm1, [rdi+xmm2*1], xmm	22	2
XED_IFORM_VPGATHERQQ_XMMu64_MASKmskw_MEMu64_AVX512_VL128	vpgatherqq xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VPGATHERQQ_YMMu64_MASKmskw_MEMu64_AVX512_VL256	vpgatherqq ymm1{k1}, [rdi+ymm2*1]	25	4

XED_IFORM_VPGATHERQQ_ZMMu64_MASKmskw_MEMu64_AVX512_VL512	vpgatherqq zmm1{k1}, [rdi+zmm2*1]	26	5
XED_IFORM_PHADDD_XMMdq_MEMdq	vphaddd xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDD_XMMdq_XMMdq	vphaddd xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHADDD_XMMdq_XMMdq_MEMdq	vphaddd xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDD_XMMdq_XMMdq_XMMdq	vphaddd xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDD_YMMqq_YMMqq_MEMqq	vphaddd ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHADDD_YMMqq_YMMqq_YMMqq	vphaddd ymm1, ymm2, ymm3	3	2
XED_IFORM_PHADDSW_XMMdq_MEMdq	vphaddsw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDSW_XMMdq_XMMdq	vphaddsw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHADDSW_XMMdq_XMMdq_MEMdq	vphaddsw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDSW_XMMdq_XMMdq_XMMdq	vphaddsw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDSW_YMMqq_YMMqq_MEMqq	vphaddsw ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHADDSW_YMMqq_YMMqq_YMMqq	vphaddsw ymm1, ymm2, ymm3	3	2
XED_IFORM_PHADDW_XMMdq_MEMdq	vphaddw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDW_XMMdq_XMMdq	vphaddw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHADDW_XMMdq_XMMdq_MEMdq	vphaddw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDW_XMMdq_XMMdq_XMMdq	vphaddw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDW_YMMqq_YMMqq_MEMqq	vphaddw ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHADDW_YMMqq_YMMqq_YMMqq	vphaddw ymm1, ymm2, ymm3	3	2
XED_IFORM_VPHMINPOSUW_XMMdq_MEMdq	vphminposuw xmm1, [rdi]	10	0.5
XED_IFORM_PHMINPOSUW_XMMdq_MEMdq	vphminposuw xmm1, [rdi]	10	0.5
XED_IFORM_PHMINPOSUW_XMMdq_XMMdq	vphminposuw xmm1, xmm2	4	0.33
XED_IFORM_VPHMINPOSUW_XMMdq_XMMdq	vphminposuw xmm1, xmm2	4	0.33
XED_IFORM_PHSUBD_XMMdq_MEMdq	vphsubd xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBD_XMMdq_XMMdq	vphsubd xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBD_XMMdq_XMMdq_MEMdq	vphsubd xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBD_XMMdq_XMMdq_XMMdq	vphsubd xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBD_YMMqq_YMMqq_MEMqq	vphsubd ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHSUBD_YMMqq_YMMqq_YMMqq	vphsubd ymm1, ymm2, ymm3	3	2
XED_IFORM_PHSUBSW_XMMdq_MEMdq	vphsubsw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBSW_XMMdq_XMMdq	vphsubsw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBSW_XMMdq_XMMdq_MEMdq	vphsubsw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBSW_XMMdq_XMMdq_XMMdq	vphsubsw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBSW_YMMqq_YMMqq_MEMqq	vphsubsw ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHSUBSW_YMMqq_YMMqq_YMMqq	vphsubsw ymm1, ymm2, ymm3	3	2
XED_IFORM_PHSUBW_XMMdq_MEMdq	vphsubw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBW_XMMdq_XMMdq	vphsubw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBW_XMMdq_XMMdq_MEMdq	vphsubw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBW_XMMdq_XMMdq_XMMdq	vphsubw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBW_YMMqq_YMMqq_MEMqq	vphsubw ymm1, ymm2, [rdi]	10	2
XED_IFORM_VPHSUBW_YMMqq_YMMqq_YMMqq	vphsubw ymm1, ymm2, ymm3	3	2

XED_IFORM_PINSRB_XMMdq_MEMb_IMMb	vpinsrb xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRB_XMMdq_GPR32d_IMMb	vpinsrb xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRB_XMMu8_XMMu8_MEMu8_IMM8_AVX512	vpinsrb xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRB_XMMdq_XMMdq_MEMb_IMMb	vpinsrb xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRB_XMMdq_XMMdq_GPR32d_IMMb	vpinsrb xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRB_XMMu8_XMMu8_GPR32u8_IMM8_AVX512	vpinsrb xmm1, xmm2, eax, 1	2	2
XED_IFORM_PINSRD_XMMdq_MEMd_IMMb	vpinsrd xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRD_XMMdq_GPR32d_IMMb	vpinsrd xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRD_XMMdq_XMMdq_MEMd_IMMb	vpinsrd xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRD_XMMu32_XMMu32_MEMu32_IMM8_AVX512	vpinsrd xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRD_XMMu32_XMMu32_GPR32u32_IMM8_AVX512	vpinsrd xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRD_XMMdq_XMMdq_GPR32d_IMMb	vpinsrd xmm1, xmm2, eax, 1	2	2
XED_IFORM_PINSRQ_XMMdq_MEMq_IMMb	vpinsrq xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRQ_XMMdq_GPR64q_IMMb	vpinsrq xmm1, xmm1, rax, 1	2	2
XED_IFORM_VPINSRQ_XMMdq_XMMdq_MEMq_IMMb	vpinsrq xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRQ_XMMu64_XMMu64_MEMu64_IMM8_AVX512	vpinsrq xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRQ_XMMdq_XMMdq_GPR64q_IMMb	vpinsrq xmm1, xmm2, rax, 1	2	2
XED_IFORM_VPINSRQ_XMMu64_XMMu64_GPR64u64_IMM8_AVX512	vpinsrq xmm1, xmm2, rax, 1	2	2
XED_IFORM_PINSRW_XMMdq_MEMw_IMMb	vpinsrw xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRW_XMMdq_GPR32_IMMb	vpinsrw xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRW_XMMu16_XMMu16_MEMu16_IMM8_AVX512	vpinsrw xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRW_XMMdq_XMMdq_MEMw_IMMb	vpinsrw xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRW_XMMu16_XMMu16_GPR32u16_IMM8_AVX512	vpinsrw xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRW_XMMdq_XMMdq_GPR32d_IMMb	vpinsrw xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPLZCNTD_XMMu32_MASKmskw_MEMu32_AVX512	vplzcntd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VPLZCNTD_XMMu32_MASKmskw_XMMu32_AVX512	vplzcntd xmm1{k1}, xmm2	4	0.5
XED_IFORM_VPLZCNTD_YMMu32_MASKmskw_MEMu32_AVX512	vplzcntd ymm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTD_YMMu32_MASKmskw_YMMu32_AVX512	vplzcntd ymm1{k1}, ymm2	4	0.5
XED_IFORM_VPLZCNTD_ZMMu32_MASKmskw_MEMu32_AVX512CD	vplzcntd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTD_ZMMu32_MASKmskw_ZMMu32_AVX512CD	vplzcntd zmm1{k1}, zmm2	4	0.5
XED_IFORM_VPLZCNTQ_XMMu64_MASKmskw_MEMu64_AVX512	vplzcntq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VPLZCNTQ_XMMu64_MASKmskw_XMMu64_AVX512	vplzcntq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VPLZCNTQ_YMMu64_MASKmskw_MEMu64_AVX512	vplzcntq ymm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTQ_YMMu64_MASKmskw_YMMu64_AVX512	vplzcntq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VPLZCNTQ_ZMMu64_MASKmskw_MEMu64_AVX512CD	vplzcntq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTQ_ZMMu64_MASKmskw_ZMMu64_AVX512CD	vplzcntq zmm1{k1}, zmm2	4	0.5
XED_IFORM_PMADDUBSW_XMMdq_MEMdq	vpmaddubsw xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMADDUBSW_XMMdq_XMMdq	vpmaddubsw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMADDUBSW_XMMdq_XMMdq_MEMdq	vpmaddubsw xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMADDUBSW_XMMdq_XMMdq_XMMdq	vpmaddubsw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDUBSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmaddubsw xmm1{k1}, xmm2, [rdi]	11	0.5

XED_IFORM_VPMADDUBSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmaddubsw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDUBSW_YMMqq_YMMqq_MEMqq	vpmaddubsw ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMADDUBSW_YMMqq_YMMqq_YMMqq	vpmaddubsw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDUBSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmaddubsw ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMADDUBSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmaddubsw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDUBSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaddubsw zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMADDUBSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaddubsw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMADDWD_XMMdq_MEMdq	vpmaddwd xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMADDWD_XMMdq_XMMdq	vpmaddwd xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMADDWD_XMMdq_XMMdq_MEMdq	vpmaddwd xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMADDWD_XMMdq_XMMdq_XMMdq	vpmaddwd xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDWD_XMMi32_MASKmskw_XMMi16_MEMi16_AVX512	vpmaddwd xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMADDWD_XMMi32_MASKmskw_XMMi16_XMMi16_AVX512	vpmaddwd xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDWD_YMMqq_YMMqq_MEMqq	vpmaddwd ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMADDWD_YMMqq_YMMqq_YMMqq	vpmaddwd ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDWD_YMMi32_MASKmskw_YMMi16_MEMi16_AVX512	vpmaddwd ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMADDWD_YMMi32_MASKmskw_YMMi16_YMMi16_AVX512	vpmaddwd ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDWD_ZMMi32_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaddwd zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMADDWD_ZMMi32_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaddwd zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_VPMASKMOVD_MEMdq_XMMdq_XMMdq	vpmaskmovd [rdi], xmm1, xmm2	6	1
XED_IFORM_VPMASKMOVD_MEMqq_YMMqq_YMMqq	vpmaskmovd [rdi], ymm1, ymm2	6	1
XED_IFORM_VPMASKMOVD_XMMdq_XMMdq_MEMdq	vpmaskmovd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMASKMOVD_YMMqq_YMMqq_MEMqq	vpmaskmovd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMASKMOVQ_MEMdq_XMMdq_XMMdq	vpmaskmovq [rdi], xmm1, xmm2	6	1
XED_IFORM_VPMASKMOVQ_MEMqq_YMMqq_YMMqq	vpmaskmovq [rdi], ymm1, ymm2	6	1
XED_IFORM_VPMASKMOVQ_XMMdq_XMMdq_MEMdq	vpmaskmovq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMASKMOVQ_YMMqq_YMMqq_MEMqq	vpmaskmovq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_PMAXSB_XMMdq_MEMdq	vpmaxsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXSB_XMMdq_XMMdq	vpmaxsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXSB_XMMdq_XMMdq_MEMdq	vpmaxsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSB_XMMdq_XMMdq_XMMdq	vpmaxsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpmaxsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpmaxsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSB_YMMqq_YMMqq_MEMqq	vpmaxsb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSB_YMMqq_YMMqq_YMMqq	vpmaxsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpmaxsb ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpmaxsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpmaxsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpmaxsb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXSD_XMMdq_MEMdq	vpmaxsd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXSD_XMMdq_XMMdq	vpmaxsd xmm1, xmm1, xmm2	1	0.5

XED_IFORM_VPMAXSD_XMMdq_XMMdq_MEMdq	vpmaxsd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSD_XMMdq_XMMdq_XMMdq	vpmaxsd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSD_XMMi32_MASKmskw_XMMi32_MEMi32_AVX512	vpmaxsd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSD_XMMi32_MASKmskw_XMMi32_XMMi32_AVX512	vpmaxsd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSD_YMMqq_YMMqq_MEMqq	vpmaxsd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSD_YMMqq_YMMqq_YMMqq	vpmaxsd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSD_YMMi32_MASKmskw_YMMi32_MEMi32_AVX512	vpmaxsd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSD_YMMi32_MASKmskw_YMMi32_YMMi32_AVX512	vpmaxsd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSD_ZMMi32_MASKmskw_ZMMi32_MEMi32_AVX512	vpmaxsd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSD_ZMMi32_MASKmskw_ZMMi32_ZMMi32_AVX512	vpmaxsd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMAXSQ_XMMi64_MASKmskw_XMMi64_MEMi64_AVX512	vpmaxsq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMAXSQ_XMMi64_MASKmskw_XMMi64_XMMi64_AVX512	vpmaxsq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMAXSQ_YMMi64_MASKmskw_YMMi64_MEMi64_AVX512	vpmaxsq ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPMAXSQ_YMMi64_MASKmskw_YMMi64_YMMi64_AVX512	vpmaxsq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMAXSQ_ZMMi64_MASKmskw_ZMMi64_MEMi64_AVX512	vpmaxsq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMAXSQ_ZMMi64_MASKmskw_ZMMi64_ZMMi64_AVX512	vpmaxsq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMAXSW_XMMdq_MEMdq	vpmaxsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXSW_XMMdq_XMMdq	vpmaxsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXSW_XMMdq_XMMdq_MEMdq	vpmaxsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSW_XMMdq_XMMdq_XMMdq	vpmaxsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmaxsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmaxsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSW_YMMqq_YMMqq_MEMqq	vpmaxsw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSW_YMMqq_YMMqq_YMMqq	vpmaxsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmaxsw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmaxsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaxsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaxsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXUB_XMMdq_MEMdq	vpmaxub xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXUB_XMMdq_XMMdq	vpmaxub xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUB_XMMdq_XMMdq_MEMdq	vpmaxub xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUB_XMMdq_XMMdq_XMMdq	vpmaxub xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpmaxub xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpmaxub xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUB_YMMqq_YMMqq_MEMqq	vpmaxub ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUB_YMMqq_YMMqq_YMMqq	vpmaxub ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpmaxub ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpmaxub ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpmaxub zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpmaxub zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXUD_XMMdq_MEMdq	vpmaxud xmm1, xmm1, [rdi]	7	0.5

XED_IFORM_PMAXUD_XMMdq_XMMdq	vpmaxud xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUD_XMMdq_XMMdq_MEMdq	vpmaxud xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUD_XMMdq_XMMdq_XMMdq	vpmaxud xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpmaxud xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpmaxud xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUD_YMMqq_YMMqq_MEMqq	vpmaxud ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUD_YMMqq_YMMqq_YMMqq	vpmaxud ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpmaxud ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpmaxud ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpmaxud zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmaxud zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMAXUQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpmaxuq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMAXUQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpmaxuq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMAXUQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpmaxuq ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPMAXUQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpmaxuq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMAXUQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpmaxuq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMAXUQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpmaxuq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMAXUW_XMMdq_MEMdq	vpmaxuw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXUW_XMMdq_XMMdq	vpmaxuw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUW_XMMdq_XMMdq_MEMdq	vpmaxuw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUW_XMMdq_XMMdq_XMMdq	vpmaxuw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmaxuw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmaxuw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUW_YMMqq_YMMqq_MEMqq	vpmaxuw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUW_YMMqq_YMMqq_YMMqq	vpmaxuw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmaxuw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMAXUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmaxuw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmaxuw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmaxuw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINSB_XMMdq_MEMdq	vpminsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSB_XMMdq_XMMdq	vpminsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSB_XMMdq_XMMdq_MEMdq	vpminsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSB_XMMdq_XMMdq_XMMdq	vpminsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpminsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpminsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSB_YMMqq_YMMqq_MEMqq	vpminsb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSB_YMMqq_YMMqq_YMMqq	vpminsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpminsb ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpminsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpminsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpminsb zmm1{k1}, zmm2, zmm3	1	1

XED_IFORM_PMINSD_XMMdq_MEMdq	vpminsd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSD_XMMdq_XMMdq	vpminsd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSD_XMMdq_XMMdq_MEMdq	vpminsd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSD_XMMdq_XMMdq_XMMdq	vpminsd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSD_XMMi32_MASKmskw_XMMi32_MEMi32_AVX512	vpminsd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSD_XMMi32_MASKmskw_XMMi32_XMMi32_AVX512	vpminsd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSD_YMMqq_YMMqq_MEMqq	vpminsd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSD_YMMqq_YMMqq_YMMqq	vpminsd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSD_YMMi32_MASKmskw_YMMi32_MEMi32_AVX512	vpminsd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSD_YMMi32_MASKmskw_YMMi32_YMMi32_AVX512	vpminsd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSD_ZMMi32_MASKmskw_ZMMi32_MEMi32_AVX512	vpminsd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSD_ZMMi32_MASKmskw_ZMMi32_ZMMi32_AVX512	vpminsd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMINSQ_XMMi64_MASKmskw_XMMi64_MEMi64_AVX512	vpminsq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMINSQ_XMMi64_MASKmskw_XMMi64_XMMi64_AVX512	vpminsq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMINSQ_YMMi64_MASKmskw_YMMi64_MEMi64_AVX512	vpminsq ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPMINSQ_YMMi64_MASKmskw_YMMi64_YMMi64_AVX512	vpminsq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMINSQ_ZMMi64_MASKmskw_ZMMi64_MEMi64_AVX512	vpminsq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMINSQ_ZMMi64_MASKmskw_ZMMi64_ZMMi64_AVX512	vpminsq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMINSW_XMMdq_MEMdq	vpminsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSW_XMMdq_XMMdq	vpminsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSW_XMMdq_XMMdq_MEMdq	vpminsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSW_XMMdq_XMMdq_XMMdq	vpminsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpminsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpminsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSW_YMMqq_YMMqq_MEMqq	vpminsw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSW_YMMqq_YMMqq_YMMqq	vpminsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpminsw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpminsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpminsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpminsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINUB_XMMdq_MEMdq	vpminub xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUB_XMMdq_XMMdq	vpminub xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUB_XMMdq_XMMdq_MEMdq	vpminub xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUB_XMMdq_XMMdq_XMMdq	vpminub xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpminub xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpminub xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUB_YMMqq_YMMqq_MEMqq	vpminub ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUB_YMMqq_YMMqq_YMMqq	vpminub ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpminub ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpminub ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpminub zmm1{k1}, zmm2, [rdi]	8	1

XED_IFORM_VPMINUB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpminub zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINUD_XMMdq_MEMdq	vpminud xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUD_XMMdq_XMMdq	vpminud xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUD_XMMdq_XMMdq_MEMdq	vpminud xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUD_XMMdq_XMMdq_XMMdq	vpminud xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpminud xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpminud xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUD_YMMqq_YMMqq_MEMqq	vpminud ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUD_YMMqq_YMMqq_YMMqq	vpminud ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpminud ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpminud ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpminud zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINUD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpminud zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMINUQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpminuq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMINUQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpminuq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMINUQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpminuq ymm1{k1}, ymm2, [rdi]	10	1
XED_IFORM_VPMINUQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpminuq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMINUQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpminuq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMINUQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpminuq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMINUW_XMMdq_MEMdq	vpminuw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUW_XMMdq_XMMdq	vpminuw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUW_XMMdq_XMMdq_MEMdq	vpminuw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUW_XMMdq_XMMdq_XMMdq	vpminuw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpminuw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpminuw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUW_YMMqq_YMMqq_MEMqq	vpminuw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUW_YMMqq_YMMqq_YMMqq	vpminuw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpminuw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPMINUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpminuw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpminuw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpminuw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMOVB2M_MASKmskw_XMMu8_AVX512	vpmovb2m k1, xmm1	1	1
XED_IFORM_VPMOVB2M_MASKmskw_YMMu8_AVX512	vpmovb2m k1, ymm1	1	1
XED_IFORM_VPMOVB2M_MASKmskw_ZMMu8_AVX512	vpmovb2m k1, zmm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_XMMu32_AVX512	vpmovd2m k1, xmm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_YMMu32_AVX512	vpmovd2m k1, ymm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_ZMMu32_AVX512	vpmovd2m k1, zmm1	1	1
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_XMMu32_AVX512	vpmovdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_YMMu32_AVX512	vpmovdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_ZMMu32_AVX512	vpmovdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVDB_XMMu8_MASKmskw_XMMu32_AVX512	vpmovdb xmm1{k1}, xmm2	4	2

XED_IFORM_VPMOVDB_XMMu8_MASKmskw_YMMu32_AVX512	vpmovdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVDB_XMMu8_MASKmskw_ZMMu32_AVX512	vpmovdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_XMMu32_AVX512	vpmovdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_YMMu32_AVX512	vpmovdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_ZMMu32_AVX512	vpmovdw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVDW_XMMu16_MASKmskw_XMMu32_AVX512	vpmovdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVDW_XMMu16_MASKmskw_YMMu32_AVX512	vpmovdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVDW_YMMu16_MASKmskw_ZMMu32_AVX512	vpmovdw ymm1{k1}, zmm2	4	2
XED_IFORM_PMOVMSKB_GPR32_XMMdq	vpmovmskb eax, xmm1	2	1
XED_IFORM_VPMOVMSKB_GPR32d_XMMdq	vpmovmskb eax, xmm1	2	1
XED_IFORM_VPMOVMSKB_GPR32d_YMMqq	vpmovmskb eax, ymm1	2	1
XED_IFORM_VPMOVQ2M_MASKmskw_XMMu64_AVX512	vpmovq2m k1, xmm1	1	1
XED_IFORM_VPMOVQ2M_MASKmskw_YMMu64_AVX512	vpmovq2m k1, ymm1	1	1
XED_IFORM_VPMOVQ2M_MASKmskw_ZMMu64_AVX512	vpmovq2m k1, zmm1	1	1
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_XMMu64_AVX512	vpmovqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_YMMu64_AVX512	vpmovqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_ZMMu64_AVX512	vpmovqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_XMMu64_AVX512	vpmovqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_YMMu64_AVX512	vpmovqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_ZMMu64_AVX512	vpmovqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_XMMu64_AVX512	vpmovqd [rdi]{k1}, xmm1	8	1
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_YMMu64_AVX512	vpmovqd [rdi]{k1}, ymm1	8	1
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_ZMMu64_AVX512	vpmovqd [rdi]{k1}, zmm1	8	1
XED_IFORM_VPMOVQD_XMMu32_MASKmskw_XMMu64_AVX512	vpmovqd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVQD_XMMu32_MASKmskw_YMMu64_AVX512	vpmovqd xmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVQD_YMMu32_MASKmskw_ZMMu64_AVX512	vpmovqd ymm1{k1}, zmm2	3	1
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_XMMu64_AVX512	vpmovqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_YMMu64_AVX512	vpmovqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_ZMMu64_AVX512	vpmovqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_XMMu64_AVX512	vpmovqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_YMMu64_AVX512	vpmovqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_ZMMu64_AVX512	vpmovqw xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_XMMi32_AVX512	vpmovsdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_YMMi32_AVX512	vpmovsdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_ZMMi32_AVX512	vpmovsdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_XMMi32_AVX512	vpmovsdb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_YMMi32_AVX512	vpmovsdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_ZMMi32_AVX512	vpmovsdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_XMMi32_AVX512	vpmovsdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_YMMi32_AVX512	vpmovsdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_ZMMi32_AVX512	vpmovsdw [rdi]{k1}, zmm1	9	2

XED_IFORM_VPMOVSDW_XMMi16_MASKmskw_XMMi32_AVX512	vpmovsdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSDW_XMMi16_MASKmskw_YMMi32_AVX512	vpmovsdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSDW_YMMi16_MASKmskw_ZMMi32_AVX512	vpmovsdw ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_XMMi64_AVX512	vpmovsqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_YMMi64_AVX512	vpmovsqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_ZMMi64_AVX512	vpmovsqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_XMMi64_AVX512	vpmovsqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_YMMi64_AVX512	vpmovsqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_ZMMi64_AVX512	vpmovsqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_XMMi64_AVX512	vpmovsqd [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_YMMi64_AVX512	vpmovsqd [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_ZMMi64_AVX512	vpmovsqd [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQD_XMMi32_MASKmskw_XMMi64_AVX512	vpmovsqd xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQD_XMMi32_MASKmskw_YMMi64_AVX512	vpmovsqd xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQD_YMMi32_MASKmskw_ZMMi64_AVX512	vpmovsqd ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_XMMi64_AVX512	vpmovsqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_YMMi64_AVX512	vpmovsqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_ZMMi64_AVX512	vpmovsqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_XMMi64_AVX512	vpmovsqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_YMMi64_AVX512	vpmovsqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_ZMMi64_AVX512	vpmovsqw xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_XMMi16_AVX512	vpmovswb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_YMMi16_AVX512	vpmovswb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_ZMMi16_AVX512	vpmovswb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSWB_XMMi8_MASKmskw_XMMi16_AVX512	vpmovswb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSWB_XMMi8_MASKmskw_YMMi16_AVX512	vpmovswb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSWB_YMMi8_MASKmskw_ZMMi16_AVX512	vpmovswb ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSXBD_XMMdq_MEMd	vpmovsxbd xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBD_XMMdq_MEMd	vpmovsxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXBD_XMMdq_XMMd	vpmovsxbd xmm1, xmm2	1	1
XED_IFORM_PMOVSXBD_XMMdq_XMMd	vpmovsxbd xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBD_XMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBD_XMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBD_YMMqq_MEMq	vpmovsxbd ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXBD_YMMqq_XMMq	vpmovsxbd ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBD_YMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBD_YMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBD_ZMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBD_ZMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd zmm1{k1}, xmm2	3	1
XED_IFORM_PMOVSXBQ_XMMdq_MEMw	vpmovsxbq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXBQ_XMMdq_MEMw	vpmovsxbq xmm1, [rdi]	6	1

XED_IFORM_VPMOVSXBQ_XMMdq_XMMw	vpmovsxbq xmm1, xmm2	1	1
XED_IFORM_PMOVSXBQ_XMMdq_XMMw	vpmovsxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBQ_XMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBQ_XMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBQ_YMMqq_MEMd	vpmovsxbq ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXBQ_YMMqq_XMMd	vpmovsxbq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBQ_YMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBQ_YMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBQ_ZMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBQ_ZMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_XMMdq_MEMq	vpmovsxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBW_XMMdq_MEMq	vpmovsxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBW_XMMdq_XMMq	vpmovsxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBW_XMMdq_XMMq	vpmovsxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBW_XMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBW_XMMi16_MASKmskw_XMMi8_AVX512	vpmovsxbw xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_YMMqq_MEMdq	vpmovsxbw ymm1, [rdi]	9	1
XED_IFORM_VPMOVSXBW_YMMqq_XMMdq	vpmovsxbw ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBW_YMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBW_YMMi16_MASKmskw_XMMi8_AVX512	vpmovsxbw ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_ZMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBW_ZMMi16_MASKmskw_YMMi8_AVX512	vpmovsxbw zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVSXDQ_XMMdq_MEMq	vpmovsxdq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXDQ_XMMdq_MEMq	vpmovsxdq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXDQ_XMMdq_XMMq	vpmovsxdq xmm1, xmm2	1	1
XED_IFORM_PMOVSXDQ_XMMdq_XMMq	vpmovsxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXDQ_XMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXDQ_XMMi64_MASKmskw_XMMi32_AVX512	vpmovsxdq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXDQ_YMMqq_MEMdq	vpmovsxdq ymm1, [rdi]	9	1
XED_IFORM_VPMOVSXDQ_YMMqq_XMMdq	vpmovsxdq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXDQ_YMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXDQ_YMMi64_MASKmskw_XMMi32_AVX512	vpmovsxdq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXDQ_ZMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXDQ_ZMMi64_MASKmskw_YMMi32_AVX512	vpmovsxdq zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVSXWD_XMMdq_MEMq	vpmovsxwd xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXWD_XMMdq_MEMq	vpmovsxwd xmm1, [rdi]	6	1
XED_IFORM_PMOVSXWD_XMMdq_XMMq	vpmovsxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWD_XMMdq_XMMq	vpmovsxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWD_XMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXWD_XMMi32_MASKmskw_XMMi16_AVX512	vpmovsxwd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWD_YMMqq_MEMdq	vpmovsxwd ymm1, [rdi]	9	1

XED_IFORM_VPMOVSXWD_YMMqq_XMMdq	vpmovsxwd ymm1, xmm2	3	1
XED_IFORM_VPMOVSXWD_YMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWD_YMMi32_MASKmskw_XMMi16_AVX512	vpmovsxwd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWD_ZMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWD_ZMMi32_MASKmskw_YMMi16_AVX512	vpmovsxwd zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVSXWQ_XMMdq_MEMd	vpmovsxwq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXWQ_XMMdq_MEMd	vpmovsxwq xmm1, [rdi]	6	1
XED_IFORM_PMOVSXWQ_XMMdq_XMMd	vpmovsxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWQ_XMMdq_XMMd	vpmovsxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWQ_XMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXWQ_XMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWQ_YMMqq_MEMq	vpmovsxwq ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXWQ_YMMqq_XMMq	vpmovsxwq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXWQ_YMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWQ_YMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWQ_ZMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWQ_ZMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_XMMu32_AVX512	vpmovusdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_YMMu32_AVX512	vpmovusdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_ZMMu32_AVX512	vpmovusdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_XMMu32_AVX512	vpmovusdb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_YMMu32_AVX512	vpmovusdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_ZMMu32_AVX512	vpmovusdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_XMMu32_AVX512	vpmovusdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_YMMu32_AVX512	vpmovusdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_ZMMu32_AVX512	vpmovusdw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSDW_XMMu16_MASKmskw_XMMu32_AVX512	vpmovusdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSDW_XMMu16_MASKmskw_YMMu32_AVX512	vpmovusdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSDW_YMMu16_MASKmskw_ZMMu32_AVX512	vpmovusdw ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_XMMu64_AVX512	vpmovusqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_YMMu64_AVX512	vpmovusqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_ZMMu64_AVX512	vpmovusqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_XMMu64_AVX512	vpmovusqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_YMMu64_AVX512	vpmovusqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_ZMMu64_AVX512	vpmovusqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_XMMu64_AVX512	vpmovusqd [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_YMMu64_AVX512	vpmovusqd [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_ZMMu64_AVX512	vpmovusqd [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQD_XMMu32_MASKmskw_XMMu64_AVX512	vpmovusqd xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQD_XMMu32_MASKmskw_YMMu64_AVX512	vpmovusqd xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQD_YMMu32_MASKmskw_ZMMu64_AVX512	vpmovusqd ymm1{k1}, zmm2	4	2

XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_XMMu64_AVX512	vpmovusqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_YMMu64_AVX512	vpmovusqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_ZMMu64_AVX512	vpmovusqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_XMMu64_AVX512	vpmovusqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_YMMu64_AVX512	vpmovusqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_ZMMu64_AVX512	vpmovusqw xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_XMMu16_AVX512	vpmovuswb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_YMMu16_AVX512	vpmovuswb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_ZMMu16_AVX512	vpmovuswb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSWB_XMMu8_MASKmskw_XMMu16_AVX512	vpmovuswb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSWB_XMMu8_MASKmskw_YMMu16_AVX512	vpmovuswb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSWB_YMMu8_MASKmskw_ZMMu16_AVX512	vpmovuswb ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVW2M_MASKmskw_XMMu16_AVX512	vpmovw2m k1, xmm1	1	1
XED_IFORM_VPMOVW2M_MASKmskw_YMMu16_AVX512	vpmovw2m k1, ymm1	1	1
XED_IFORM_VPMOVW2M_MASKmskw_ZMMu16_AVX512	vpmovw2m k1, zmm1	1	1
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_XMMu16_AVX512	vpmovwb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_YMMu16_AVX512	vpmovwb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_ZMMu16_AVX512	vpmovwb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVWB_XMMu8_MASKmskw_XMMu16_AVX512	vpmovwb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVWB_XMMu8_MASKmskw_YMMu16_AVX512	vpmovwb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVWB_YMMu8_MASKmskw_ZMMu16_AVX512	vpmovwb ymm1{k1}, zmm2	4	2
XED_IFORM_PMOVZXBD_XMMdq_MEMd	vpmovzxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBD_XMMdq_MEMd	vpmovzxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBD_XMMdq_XMMd	vpmovzxbd xmm1, xmm2	1	1
XED_IFORM_PMOVZXBD_XMMdq_XMMd	vpmovzxbd xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBD_XMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXBD_XMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBD_YMMqq_MEMq	vpmovzxbd ymm1, [rdi]	10	1
XED_IFORM_VPMOVZXBD_YMMqq_XMMq	vpmovzxbd ymm1, xmm2	3	1
XED_IFORM_VPMOVZXBD_YMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBD_YMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBD_ZMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBD_ZMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd zmm1{k1}, xmm2	3	1
XED_IFORM_PMOVZXBQ_XMMdq_MEMw	vpmovzxbq xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBQ_XMMdq_MEMw	vpmovzxbq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXBQ_XMMdq_XMMw	vpmovzxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBQ_XMMdq_XMMw	vpmovzxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBQ_XMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXBQ_XMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBQ_YMMqq_MEMd	vpmovzxbq ymm1, [rdi]	10	1
XED_IFORM_VPMOVZXBQ_YMMqq_XMMd	vpmovzxbq ymm1, xmm2	3	1

XED_IFORM_VPMOVZXBQ_YMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBQ_YMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBQ_ZMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBQ_ZMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_XMMdq_MEMq	vpmovzxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVZXBW_XMMdq_MEMq	vpmovzxbw xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBW_XMMdq_XMMq	vpmovzxbw xmm1, xmm2	1	1
XED_IFORM_PMOVZXBW_XMMdq_XMMq	vpmovzxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBW_XMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXBW_XMMi16_MASKmskw_XMMi8_AVX512	vpmovzxbw xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_YMMqq_MEMdq	vpmovzxbw ymm1, [rdi]	10	1
XED_IFORM_VPMOVZXBW_YMMqq_XMMdq	vpmovzxbw ymm1, xmm2	3	1
XED_IFORM_VPMOVZXBW_YMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBW_YMMi16_MASKmskw_XMMi8_AVX512	vpmovzxbw ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_ZMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBW_ZMMi16_MASKmskw_YMMi8_AVX512	vpmovzxbw zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVZXDQ_XMMdq_MEMq	vpmovzxdq xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXDQ_XMMdq_MEMq	vpmovzxdq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXDQ_XMMdq_XMMq	vpmovzxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXDQ_XMMdq_XMMq	vpmovzxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXDQ_XMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXDQ_XMMi64_MASKmskw_XMMi32_AVX512	vpmovzxdq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXDQ_YMMqq_MEMdq	vpmovzxdq ymm1, [rdi]	10	1
XED_IFORM_VPMOVZXDQ_YMMqq_XMMdq	vpmovzxdq ymm1, xmm2	3	1
XED_IFORM_VPMOVZXDQ_YMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXDQ_YMMi64_MASKmskw_XMMi32_AVX512	vpmovzxdq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXDQ_ZMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXDQ_ZMMi64_MASKmskw_YMMi32_AVX512	vpmovzxdq zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVZXWD_XMMdq_MEMq	vpmovzxwd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXWD_XMMdq_MEMq	vpmovzxwd xmm1, [rdi]	6	1
XED_IFORM_PMOVZXWD_XMMdq_XMMq	vpmovzxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWD_XMMdq_XMMq	vpmovzxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWD_XMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXWD_XMMi32_MASKmskw_XMMi16_AVX512	vpmovzxwd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWD_YMMqq_MEMdq	vpmovzxwd ymm1, [rdi]	9	1
XED_IFORM_VPMOVZXWD_YMMqq_XMMdq	vpmovzxwd ymm1, xmm2	3	1
XED_IFORM_VPMOVZXWD_YMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWD_YMMi32_MASKmskw_XMMi16_AVX512	vpmovzxwd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWD_ZMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWD_ZMMi32_MASKmskw_YMMi16_AVX512	vpmovzxwd zmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVZXWQ_XMMdq_MEMd	vpmovzxwq xmm1, [rdi]	6	1

XED_IFORM_PMOVZXWQ_XMMdq_MEMd	vpmovzxwq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXWQ_XMMdq_XMMd	vpmovzxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWQ_XMMdq_XMMd	vpmovzxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWQ_XMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXWQ_XMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWQ_YMMqq_MEMq	vpmovzxwq ymm1, [rdi]	10	1
XED_IFORM_VPMOVZXWQ_YMMqq_XMMq	vpmovzxwq ymm1, xmm2	3	1
XED_IFORM_VPMOVZXWQ_YMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq ymm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWQ_YMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWQ_ZMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWQ_ZMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq zmm1{k1}, xmm2	3	1
XED_IFORM_PMULDQ_XMMdq_MEMdq	vpmuldq xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULDQ_XMMdq_XMMdq	vpmuldq xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULDQ_XMMdq_XMMdq_MEMdq	vpmuldq xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULDQ_XMMdq_XMMdq_XMMdq	vpmuldq xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULDQ_XMMi64_MASKmskw_XMMi32_MEMi32_AVX512	vpmuldq xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULDQ_XMMi64_MASKmskw_XMMi32_XMMi32_AVX512	vpmuldq xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULDQ_YMMqq_YMMqq_MEMqq	vpmuldq ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULDQ_YMMqq_YMMqq_YMMqq	vpmuldq ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULDQ_YMMi64_MASKmskw_YMMi32_MEMi32_AVX512	vpmuldq ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULDQ_YMMi64_MASKmskw_YMMi32_YMMi32_AVX512	vpmuldq ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULDQ_ZMMi64_MASKmskw_ZMMi32_MEMi32_AVX512	vpmuldq zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULDQ_ZMMi64_MASKmskw_ZMMi32_ZMMi32_AVX512	vpmuldq zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULHRSW_XMMdq_MEMdq	vpmulhrsw xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULHRSW_XMMdq_XMMdq	vpmulhrsw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHRSW_XMMdq_XMMdq_MEMdq	vpmulhrsw xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHRSW_XMMdq_XMMdq_XMMdq	vpmulhrsw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHRSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmulhrsw xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHRSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmulhrsw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHRSW_YMMqq_YMMqq_MEMqq	vpmulhrsw ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHRSW_YMMqq_YMMqq_YMMqq	vpmulhrsw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHRSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmulhrsw ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHRSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmulhrsw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHRSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmulhrsw zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULHRSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmulhrsw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULHUW_XMMdq_MEMdq	vpmulhuw xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULHUW_XMMdq_XMMdq	vpmulhuw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHUW_XMMdq_XMMdq_MEMdq	vpmulhuw xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHUW_XMMdq_XMMdq_XMMdq	vpmulhuw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmulhuw xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmulhuw xmm1{k1}, xmm2, xmm3	5	0.5

XED_IFORM_VPMULHUW_YMMqq_YMMqq_MEMqq	vpmulhuw ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHUW_YMMqq_YMMqq_YMMqq	vpmulhuw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmulhuw ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmulhuw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmulhuw zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULHUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmulhuw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULHW_XMMdq_MEMdq	vpmulhw xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULHW_XMMdq_XMMdq	vpmulhw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHW_XMMdq_XMMdq_MEMdq	vpmulhw xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHW_XMMdq_XMMdq_XMMdq	vpmulhw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmulhw xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULHW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmulhw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHW_YMMqq_YMMqq_MEMqq	vpmulhw ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHW_YMMqq_YMMqq_YMMqq	vpmulhw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmulhw ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULHW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmulhw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmulhw zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULHW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmulhw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULLD_XMMdq_MEMdq	vpmulld xmm1, xmm1, [rdi]	16	0.66
XED_IFORM_PMULLD_XMMdq_XMMdq	vpmulld xmm1, xmm1, xmm2	10	0.66
XED_IFORM_VPMULLD_XMMdq_XMMdq_MEMdq	vpmulld xmm1, xmm2, [rdi]	16	0.66
XED_IFORM_VPMULLD_XMMdq_XMMdq_XMMdq	vpmulld xmm1, xmm2, xmm3	10	0.66
XED_IFORM_VPMULLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpmulld xmm1{k1}, xmm2, [rdi]	16	0.66
XED_IFORM_VPMULLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpmulld xmm1{k1}, xmm2, xmm3	10	0.66
XED_IFORM_VPMULLD_YMMqq_YMMqq_MEMqq	vpmulld ymm1, ymm2, [rdi]	17	0.66
XED_IFORM_VPMULLD_YMMqq_YMMqq_YMMqq	vpmulld ymm1, ymm2, ymm3	10	0.66
XED_IFORM_VPMULLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpmulld ymm1{k1}, ymm2, [rdi]	17	0.66
XED_IFORM_VPMULLD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpmulld ymm1{k1}, ymm2, ymm3	10	0.66
XED_IFORM_VPMULLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpmulld zmm1{k1}, zmm2, [rdi]	17	1
XED_IFORM_VPMULLD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmulld zmm1{k1}, zmm2, zmm3	10	1
XED_IFORM_VPMULLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpmullq xmm1{k1}, xmm2, [rdi]	11	1
XED_IFORM_VPMULLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpmullq xmm1{k1}, xmm2, xmm3	5	1
XED_IFORM_VPMULLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpmullq ymm1{k1}, ymm2, [rdi]	12	1
XED_IFORM_VPMULLQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpmullq ymm1{k1}, ymm2, ymm3	5	1
XED_IFORM_VPMULLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpmullq zmm1{k1}, zmm2, [rdi]	12	1.5
XED_IFORM_VPMULLQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpmullq zmm1{k1}, zmm2, zmm3	5	1.5
XED_IFORM_PMULLW_XMMdq_MEMdq	vpmullw xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULLW_XMMdq_XMMdq	vpmullw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULLW_XMMdq_XMMdq_MEMdq	vpmullw xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULLW_XMMdq_XMMdq_XMMdq	vpmullw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmullw xmm1{k1}, xmm2, [rdi]	11	0.5

XED_IFORM_VPMULLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmullw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULLW_YMMqq_YMMqq_MEMqq	vpmullw ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULLW_YMMqq_YMMqq_YMMqq	vpmullw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmullw ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULLW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmullw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmullw zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULLW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmullw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULUDQ_XMMdq_MEMdq	vpmuludq xmm1, xmm1, [rdi]	11	0.5
XED_IFORM_PMULUDQ_XMMdq_XMMdq	vpmuludq xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULUDQ_XMMdq_XMMdq_MEMdq	vpmuludq xmm1, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULUDQ_XMMdq_XMMdq_XMMdq	vpmuludq xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULUDQ_XMMu64_MASKmskw_XMMu32_MEMu32_AVX512	vpmuludq xmm1{k1}, xmm2, [rdi]	11	0.5
XED_IFORM_VPMULUDQ_XMMu64_MASKmskw_XMMu32_XMMu32_AVX512	vpmuludq xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULUDQ_YMMqq_YMMqq_MEMqq	vpmuludq ymm1, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULUDQ_YMMqq_YMMqq_YMMqq	vpmuludq ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULUDQ_YMMu64_MASKmskw_YMMu32_MEMu32_AVX512	vpmuludq ymm1{k1}, ymm2, [rdi]	12	0.5
XED_IFORM_VPMULUDQ_YMMu64_MASKmskw_YMMu32_YMMu32_AVX512	vpmuludq ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULUDQ_ZMMu64_MASKmskw_ZMMu32_MEMu32_AVX512	vpmuludq zmm1{k1}, zmm2, [rdi]	12	0.5
XED_IFORM_VPMULUDQ_ZMMu64_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmuludq zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_POR_XMMdq_MEMdq	vpor xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_POR_XMMdq_XMMdq	vpor xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPOR_XMMdq_XMMdq_MEMdq	vpor xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPOR_XMMdq_XMMdq_XMMdq	vpor xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPOR_YMMqq_YMMqq_MEMqq	vpor ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPOR_YMMqq_YMMqq_YMMqq	vpor ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPORD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpord xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPORD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpord xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPORD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpord ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPORD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpord ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPORD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpord zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPORD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpord zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPORQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vporq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPORQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vporq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPORQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vporq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPORQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vporq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPORQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vporq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPORQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vporq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPROLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPROLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vprold xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPROLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPROLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vprold ymm1{k1}, ymm2, 1	1	0.5

XED_IFORM_VPROLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPROLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vprold zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPROLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPROLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vprolq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPROLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPROLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vprolq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPROLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPROLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vprolq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPROLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vprolvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPROLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vprolvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPROLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vprolvd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPROLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vprolvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPROLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vprolvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPROLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vprolvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPROLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vprolvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPROLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vprolvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPROLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vprolvq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPROLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vprolvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPROLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vprolvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPROLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vprolvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPRORD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPRORD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vprord xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPRORD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPRORD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vprord ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPRORD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPRORD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vprord zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPRORQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPRORQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vprorq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPRORQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPRORQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vprorq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPRORQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPRORQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vprorq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPRORVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vprorvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPRORVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vprorvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPRORVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vprorvd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPRORVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vprorvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPRORVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vprorvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPRORVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vprorvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPRORVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vprorvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPRORVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vprorvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPRORVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vprorvq ymm1{k1}, ymm2, [rdi]	8	0.5

XED_IFORM_VPRORVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vprorvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPRORVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vprorvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPRORVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vprorvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSADBW_XMMdq_MEMdq	vpsadbw xmm1, xmm1, [rdi]	9	1
XED_IFORM_PSADBW_XMMdq_XMMdq	vpsadbw xmm1, xmm1, xmm2	3	1
XED_IFORM_VPSADBW_XMMdq_XMMdq_MEMdq	vpsadbw xmm1, xmm2, [rdi]	9	1
XED_IFORM_VPSADBW_XMMu16_XMMu8_MEMu8_AVX512	vpsadbw xmm1, xmm2, [rdi]	9	1
XED_IFORM_VPSADBW_XMMdq_XMMdq_XMMdq	vpsadbw xmm1, xmm2, xmm3	3	1
XED_IFORM_VPSADBW_XMMu16_XMMu8_XMMu8_AVX512	vpsadbw xmm1, xmm2, xmm3	3	1
XED_IFORM_VPSADBW_YMMu16_YMMu8_MEMu8_AVX512	vpsadbw ymm1, ymm2, [rdi]	10	1
XED_IFORM_VPSADBW_YMMqq_YMMqq_MEMqq	vpsadbw ymm1, ymm2, [rdi]	10	1
XED_IFORM_VPSADBW_YMMqq_YMMqq_YMMqq	vpsadbw ymm1, ymm2, ymm3	3	1
XED_IFORM_VPSADBW_YMMu16_YMMu8_YMMu8_AVX512	vpsadbw ymm1, ymm2, ymm3	3	1
XED_IFORM_VPSADBW_ZMMu16_ZMMu8_MEMu8_AVX512	vpsadbw zmm1, zmm2, [rdi]	10	1
XED_IFORM_VPSADBW_ZMMu16_ZMMu8_ZMMu8_AVX512	vpsadbw zmm1, zmm2, zmm3	3	1
XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_XMMu32_AVX512_VL128	vpscatterdd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_YMMu32_AVX512_VL256	vpscatterdd [rdi+ymm1*1]{k1}, ymm2	12	8
XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_ZMMu32_AVX512_VL512	vpscatterdd [rdi+zmm1*1]{k1}, zmm2	12	16.75
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_XMMu64_AVX512_VL128	vpscatterdq [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_YMMu64_AVX512_VL256	vpscatterdq [rdi+xmm1*1]{k1}, ymm2	11	4
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_ZMMu64_AVX512_VL512	vpscatterdq [rdi+ymm1*1]{k1}, zmm2	11	8
XED_IFORM_VPSCATTERQD_MEMu32_MASKmskw_XMMu32_AVX512_VL128	vpscatterqd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERQD_MEMu32_MASKmskw_XMMu32_AVX512_VL256	vpscatterqd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_XMMu64_AVX512_VL128	vpscatterqq [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_YMMu64_AVX512_VL256	vpscatterqq [rdi+ymm1*1]{k1}, ymm2	11	4
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_ZMMu64_AVX512_VL512	vpscatterqq [rdi+zmm1*1]{k1}, zmm2	11	8
XED_IFORM_PSHUFB_XMMdq_MEMdq	vpshufb xmm1, xmm1, [rdi]	7	1
XED_IFORM_PSHUFB_XMMdq_XMMdq	vpshufb xmm1, xmm1, xmm2	1	1
XED_IFORM_VPSHUFB_XMMdq_XMMdq_MEMdq	vpshufb xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPSHUFB_XMMdq_XMMdq_XMMdq	vpshufb xmm1, xmm2, xmm3	1	1
XED_IFORM_VPSHUFB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpshufb xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPSHUFB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpshufb xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPSHUFB_YMMqq_YMMqq_MEMqq	vpshufb ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPSHUFB_YMMqq_YMMqq_YMMqq	vpshufb ymm1, ymm2, ymm3	1	1
XED_IFORM_VPSHUFB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpshufb ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPSHUFB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpshufb ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPSHUFB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpshufb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSHUFB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpshufb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSHUFD_XMMdq_MEMdq_IMMb	vpshufd xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFD_XMMdq_MEMdq_IMMb	vpshufd xmm1, [rdi], 1	7	1
XED_IFORM_VPSHUFD_XMMdq_XMMdq_IMMb	vpshufd xmm1, xmm2, 1	1	1

XED_IFORM_PSHUFD_XMMdq_XMMdq_IMMb	vpshufd xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpshufd xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFD_YMMqq_MEMqq_IMMb	vpshufd ymm1, [rdi], 1	8	1
XED_IFORM_VPSHUFD_YMMqq_YMMqq_IMMb	vpshufd ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpshufd ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpshufd zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSHUFHW_XMMdq_MEMdq_IMMb	vpshufhw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFHW_XMMdq_MEMdq_IMMb	vpshufhw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFHW_XMMdq_XMMdq_IMMb	vpshufhw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_XMMdq_XMMdq_IMMb	vpshufhw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFHW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpshufhw xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_YMMqq_MEMqq_IMMb	vpshufhw ymm1, [rdi], 1	8	1
XED_IFORM_VPSHUFHW_YMMqq_YMMqq_IMMb	vpshufhw ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFHW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFHW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpshufhw ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFHW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFHW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpshufhw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSHUFLW_XMMdq_MEMdq_IMMb	vpshuflw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFLW_XMMdq_MEMdq_IMMb	vpshuflw xmm1, [rdi], 1	7	1
XED_IFORM_VPSHUFLW_XMMdq_XMMdq_IMMb	vpshuflw xmm1, xmm2, 1	1	1
XED_IFORM_PSHUFLW_XMMdq_XMMdq_IMMb	vpshuflw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpshuflw xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFLW_YMMqq_MEMqq_IMMb	vpshuflw ymm1, [rdi], 1	8	1
XED_IFORM_VPSHUFLW_YMMqq_YMMqq_IMMb	vpshuflw ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpshuflw ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpshuflw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_PSIGNB_XMMdq_MEMdq	vpsignb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGNB_XMMdq_XMMdq	vpsignb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSIGNB_XMMdq_XMMdq_MEMdq	vpsignb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGNB_XMMdq_XMMdq_XMMdq	vpsignb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGNB_YMMqq_YMMqq_MEMqq	vpsignb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSIGNB_YMMqq_YMMqq_YMMqq	vpsignb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSIGND_XMMdq_MEMdq	vpsignd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGND_XMMdq_XMMdq	vpsignd xmm1, xmm1, xmm2	1	0.5

XED_IFORM_VPSIGND_XMMdq_XMMdq_MEMdq	vpsignd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGND_XMMdq_XMMdq_XMMdq	vpsignd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGND_YMMqq_YMMqq_MEMqq	vpsignd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSIGND_YMMqq_YMMqq_YMMqq	vpsignd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSIGNW_XMMdq_MEMdq	vpsignw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGNW_XMMdq_XMMdq	vpsignw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSIGNW_XMMdq_XMMdq_MEMdq	vpsignw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGNW_XMMdq_XMMdq_XMMdq	vpsignw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGNW_YMMqq_YMMqq_MEMqq	vpsignw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSIGNW_YMMqq_YMMqq_YMMqq	vpsignw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSLLD_XMMdq_MEMdq	vpslld xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSLLD_XMMdq_IMMb	vpslld xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLD_XMMdq_XMMdq	vpslld xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLD_XMMdq_XMMdq_MEMdq	vpslld xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLD_XMMdq_XMMdq_IMMb	vpslld xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLD_XMMdq_XMMdq_XMMdq	vpslld xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSLLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpslld xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpslld xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpslld xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLD_YMMqq_YMMqq_MEMdq	vpslld ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLD_YMMqq_YMMqq_IMMb	vpslld ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLD_YMMqq_YMMqq_XMMq	vpslld ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpslld ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpslld ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpslld ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpslld zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpslld zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpslld zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSLLDQ_XMMu8_MEMu8_IMM8_AVX512	vpslldq xmm1, [rdi], 1	7	1
XED_IFORM_PSLLDQ_XMMdq_IMMb	vpslldq xmm1, xmm1, 1	1	1
XED_IFORM_VPSLLDQ_XMMu8_XMMu8_IMM8_AVX512	vpslldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSLLDQ_XMMdq_XMMdq_IMMb	vpslldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSLLDQ_YMMu8_MEMu8_IMM8_AVX512	vpslldq ymm1, [rdi], 1	8	1
XED_IFORM_VPSLLDQ_YMMqq_YMMqq_IMMb	vpslldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSLLDQ_YMMu8_YMMu8_IMM8_AVX512	vpslldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSLLDQ_ZMMu8_MEMu8_IMM8_AVX512	vpslldq zmm1, [rdi], 1	8	1
XED_IFORM_VPSLLDQ_ZMMu8_ZMMu8_IMM8_AVX512	vpslldq zmm1, zmm2, 1	1	1
XED_IFORM_PSLLQ_XMMdq_MEMdq	vpsllq xmm1, xmm1, [rdi]	7	0.5

XED_IFORM_PSLLQ_XMMdq_IMMb	vpsllq xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLQ_XMMdq_XMMdq	vpsllq xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLQ_XMMdq_XMMdq_MEMdq	vpsllq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLQ_XMMdq_XMMdq_IMMb	vpsllq xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLQ_XMMdq_XMMdq_XMMdq	vpsllq xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsllq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsllq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsllq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLQ_YMMqq_YMMqq_MEMdq	vpsllq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLQ_YMMqq_YMMqq_IMMb	vpsllq ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLQ_YMMqq_YMMqq_XMMq	vpsllq ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsllq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsllq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsllq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsllq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsllq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsllq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSLLVD_XMMdq_XMMdq_MEMdq	vpsllvd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVD_XMMdq_XMMdq_XMMdq	vpsllvd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsllvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsllvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVD_YMMqq_YMMqq_MEMqq	vpsllvd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLVD_YMMqq_YMMqq_YMMqq	vpsllvd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsllvd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsllvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsllvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsllvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSLLVQ_XMMdq_XMMdq_MEMdq	vpsllvq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVQ_XMMdq_XMMdq_XMMdq	vpsllvq xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsllvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsllvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVQ_YMMqq_YMMqq_MEMqq	vpsllvq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLVQ_YMMqq_YMMqq_YMMqq	vpsllvq ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsllvq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsllvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsllvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsllvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSLLVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsllvw xmm1{k1}, xmm2, [rdi]	7	0.5

XED_IFORM_VPSLLVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsllvw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsllvw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsllvw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsllvw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsllvw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSLLW_XMMdq_MEMdq	vpsllw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSLLW_XMMdq_IMMb	vpsllw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLW_XMMdq_XMMdq	vpsllw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLW_XMMdq_XMMdq_MEMdq	vpsllw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLW_XMMdq_XMMdq_IMMb	vpsllw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLW_XMMdq_XMMdq_XMMdq	vpsllw xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSLLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsllw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsllw xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsllw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLW_YMMqq_YMMqq_MEMdq	vpsllw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLW_YMMqq_YMMqq_IMMb	vpsllw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLW_YMMqq_YMMqq_XMMq	vpsllw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsllw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsllw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsllw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsllw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsllw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsllw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSRAD_XMMdq_MEMdq	vpsrad xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRAD_XMMdq_IMMb	vpsrad xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRAD_XMMdq_XMMdq	vpsrad xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRAD_XMMdq_XMMdq_MEMdq	vpsrad xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAD_XMMdq_XMMdq_IMMb	vpsrad xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRAD_XMMdq_XMMdq_XMMdq	vpsrad xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRAD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrad xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpsrad xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrad xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAD_YMMqq_YMMqq_MEMdq	vpsrad ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAD_YMMqq_YMMqq_IMMb	vpsrad ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRAD_YMMqq_YMMqq_XMMq	vpsrad ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRAD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrad ymm1{k1}, ymm2, [rdi]	8	0.5

XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpsrad ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpsrad ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrad zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpsrad zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpsrad zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsraq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsraq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsraq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsraq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsraq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsraq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsraq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsraq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsraq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRAVD_XMMdq_XMMdq_MEMdq	vpsravd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVD_XMMdq_XMMdq_XMMdq	vpsravd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsravd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsravd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVD_YMMqq_YMMqq_MEMqq	vpsravd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAVD_YMMqq_YMMqq_YMMqq	vpsravd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsravd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsravd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsravd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsravd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRAVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsravq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsravq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsravq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsravq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsravq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsravq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRAVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsravw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsravw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsravw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsravw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsravw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsravw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSRAW_XMMdq_MEMdq	vpsraw xmm1, xmm1, [rdi]	7	0.5

XED_IFORM_PSRAW_XMMdq_IMMb	vpsraw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRAW_XMMdq_XMMdq	vpsraw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRAW_XMMdq_XMMdq_MEMdq	vpsraw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAW_XMMdq_XMMdq_IMMb	vpsraw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRAW_XMMdq_XMMdq_XMMdq	vpsraw xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRAW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsraw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsraw xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsraw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAW_YMMqq_YMMqq_MEMdq	vpsraw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAW_YMMqq_YMMqq_IMMb	vpsraw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRAW_YMMqq_YMMqq_XMMq	vpsraw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRAW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsraw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsraw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsraw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsraw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsraw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsraw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSRLD_XMMdq_MEMdq	vpsrld xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLD_XMMdq_IMMb	vpsrld xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLD_XMMdq_XMMdq	vpsrld xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLD_XMMdq_XMMdq_MEMdq	vpsrld xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLD_XMMdq_XMMdq_IMMb	vpsrld xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLD_XMMdq_XMMdq_XMMdq	vpsrld xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrld xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpsrld xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrld xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLD_YMMqq_YMMqq_MEMdq	vpsrld ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLD_YMMqq_YMMqq_IMMb	vpsrld ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLD_YMMqq_YMMqq_XMMq	vpsrld ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrld ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpsrld ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpsrld ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrld zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpsrld zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpsrld zmm1{k1}, zmm2, xmm3	4	1

XED_IFORM_VPSRLDQ_XMMu8_MEMu8_IMM8_AVX512	vpsrldq xmm1, [rdi], 1	7	1
XED_IFORM_PSRLDQ_XMMdq_IMMb	vpsrldq xmm1, xmm1, 1	1	1
XED_IFORM_VPSRLDQ_XMMu8_XMMu8_IMM8_AVX512	vpsrldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSRLDQ_XMMdq_XMMdq_IMMb	vpsrldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSRLDQ_YMMu8_MEMu8_IMM8_AVX512	vpsrldq ymm1, [rdi], 1	8	1
XED_IFORM_VPSRLDQ_YMMu8_YMMu8_IMM8_AVX512	vpsrldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSRLDQ_YMMqq_YMMqq_IMMb	vpsrldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSRLDQ_ZMMu8_MEMu8_IMM8_AVX512	vpsrldq zmm1, [rdi], 1	8	1
XED_IFORM_VPSRLDQ_ZMMu8_ZMMu8_IMM8_AVX512	vpsrldq zmm1, zmm2, 1	1	1
XED_IFORM_PSRLQ_XMMdq_MEMdq	vpsrlq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLQ_XMMdq_IMMb	vpsrlq xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLQ_XMMdq_XMMdq	vpsrlq xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLQ_XMMdq_XMMdq_MEMdq	vpsrlq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLQ_XMMdq_XMMdq_IMMb	vpsrlq xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLQ_XMMdq_XMMdq_XMMdq	vpsrlq xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsrlq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsrlq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsrlq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLQ_YMMqq_YMMqq_MEMdq	vpsrlq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLQ_YMMqq_YMMqq_IMMb	vpsrlq ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLQ_YMMqq_YMMqq_XMMq	vpsrlq ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsrlq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsrlq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsrlq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsrlq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsrlq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsrlq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRLVD_XMMdq_XMMdq_MEMdq	vpsrlvd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVD_XMMdq_XMMdq_XMMdq	vpsrlvd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrlvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrlvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVD_YMMqq_YMMqq_MEMqq	vpsrlvd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLVD_YMMqq_YMMqq_YMMqq	vpsrlvd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrlvd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsrlvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrlvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsrlvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRLVQ_XMMdq_XMMdq_MEMdq	vpsrlvq xmm1, xmm2, [rdi]	7	0.5

XED_IFORM_VPSRLVQ_XMMdq_XMMdq_XMMdq	vpsrlvq xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsrlvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsrlvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVQ_YMMqq_YMMqq_MEMqq	vpsrlvq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLVQ_YMMqq_YMMqq_YMMqq	vpsrlvq ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsrlvq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsrlvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsrlvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsrlvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRLVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsrlvw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsrlvw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsrlvw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsrlvw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsrlvw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsrlvw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSRLW_XMMdq_MEMdq	vpsrlw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLW_XMMdq_IMMb	vpsrlw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLW_XMMdq_XMMdq	vpsrlw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLW_XMMdq_XMMdq_MEMdq	vpsrlw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLW_XMMdq_XMMdq_IMMb	vpsrlw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLW_XMMdq_XMMdq_XMMdq	vpsrlw xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsrlw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsrlw xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsrlw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLW_YMMqq_YMMqq_MEMdq	vpsrlw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLW_YMMqq_YMMqq_IMMb	vpsrlw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLW_YMMqq_YMMqq_XMMq	vpsrlw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw ymm1{k1}, [rdi], 1	8	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsrlw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsrlw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsrlw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsrlw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsrlw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsrlw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSUBB_XMMdq_MEMdq	vpsubb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBB_XMMdq_XMMdq	vpsubb xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBB_XMMdq_XMMdq_MEMdq	vpsubb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBB_XMMdq_XMMdq_XMMdq	vpsubb xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpsubb xmm1{k1}, xmm2, [rdi]	7	0.5

XED_IFORM_VPSUBB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpsubb xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBB_YMMqq_YMMqq_MEMqq	vpsubb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBB_YMMqq_YMMqq_YMMqq	vpsubb ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpsubb ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpsubb ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpsubb zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpsubb zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBD_XMMdq_MEMdq	vpsubd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBD_XMMdq_XMMdq	vpsubd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBD_XMMdq_XMMdq_MEMdq	vpsubd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBD_XMMdq_XMMdq_XMMdq	vpsubd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsubd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsubd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBD_YMMqq_YMMqq_MEMqq	vpsubd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBD_YMMqq_YMMqq_YMMqq	vpsubd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsubd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsubd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsubd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsubd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBQ_XMMdq_MEMdq	vpsubq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBQ_XMMdq_XMMdq	vpsubq xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBQ_XMMdq_XMMdq_MEMdq	vpsubq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBQ_XMMdq_XMMdq_XMMdq	vpsubq xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsubq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsubq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBQ_YMMqq_YMMqq_MEMqq	vpsubq ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBQ_YMMqq_YMMqq_YMMqq	vpsubq ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsubq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsubq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsubq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsubq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBSB_XMMdq_MEMdq	vpsubsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBSB_XMMdq_XMMdq	vpsubsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBSB_XMMdq_XMMdq_MEMdq	vpsubsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSB_XMMdq_XMMdq_XMMdq	vpsubsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpsubsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpsubsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSB_YMMqq_YMMqq_MEMqq	vpsubsb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBSB_YMMqq_YMMqq_YMMqq	vpsubsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpsubsb ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpsubsb ymm1{k1}, ymm2, ymm3	1	0.5

XED_IFORM_VPSUBSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpsubsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpsubsb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBSW_XMMdq_MEMdq	vpsubsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBSW_XMMdq_XMMdq	vpsubsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBSW_XMMdq_XMMdq_MEMdq	vpsubsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSW_XMMdq_XMMdq_XMMdq	vpsubsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpsubsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpsubsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSW_YMMqq_YMMqq_MEMqq	vpsubsw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBSW_YMMqq_YMMqq_YMMqq	vpsubsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpsubsw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpsubsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpsubsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpsubsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBUSB_XMMdq_MEMdq	vpsubusb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBUSB_XMMdq_XMMdq	vpsubusb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBUSB_XMMdq_XMMdq_MEMdq	vpsubusb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSB_XMMdq_XMMdq_XMMdq	vpsubusb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpsubusb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpsubusb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSB_YMMqq_YMMqq_MEMqq	vpsubusb ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBUSB_YMMqq_YMMqq_YMMqq	vpsubusb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpsubusb ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBUSB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpsubusb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpsubusb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBUSB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpsubusb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBUSW_XMMdq_MEMdq	vpsubusw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBUSW_XMMdq_XMMdq	vpsubusw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBUSW_XMMdq_XMMdq_MEMdq	vpsubusw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSW_XMMdq_XMMdq_XMMdq	vpsubusw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsubusw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsubusw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSW_YMMqq_YMMqq_MEMqq	vpsubusw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBUSW_YMMqq_YMMqq_YMMqq	vpsubusw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsubusw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBUSW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsubusw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsubusw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBUSW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsubusw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBW_XMMdq_MEMdq	vpsubw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBW_XMMdq_XMMdq	vpsubw xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBW_XMMdq_XMMdq_MEMdq	vpsubw xmm1, xmm2, [rdi]	7	0.5

XED_IFORM_VPSUBW_XMMdq_XMMdq_XMMdq	vpsubw xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsubw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsubw xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBW_YMMqq_YMMqq_MEMqq	vpsubw ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBW_YMMqq_YMMqq_YMMqq	vpsubw ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsubw ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPSUBW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsubw ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsubw zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsubw zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPTERNLOGD_XMMu32_MASKmskw_XMMu32_MEMu32_IMM8_AVX512	vpternlogd xmm1{k1}, xmm2, [rdi], 1	7	0.5
XED_IFORM_VPTERNLOGD_XMMu32_MASKmskw_XMMu32_XMMu32_IMM8_AVX512	vpternlogd xmm1{k1}, xmm2, xmm3, 1	1	0.33
XED_IFORM_VPTERNLOGD_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vpternlogd ymm1{k1}, ymm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGD_YMMu32_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vpternlogd ymm1{k1}, ymm2, ymm3, 1	1	0.33
XED_IFORM_VPTERNLOGD_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vpternlogd zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vpternlogd zmm1{k1}, zmm2, zmm3, 1	1	0.5
XED_IFORM_VPTERNLOGQ_XMMu64_MASKmskw_XMMu64_MEMu64_IMM8_AVX512	vpternlogq xmm1{k1}, xmm2, [rdi], 1	7	0.5
XED_IFORM_VPTERNLOGQ_XMMu64_MASKmskw_XMMu64_XMMu64_IMM8_AVX512	vpternlogq xmm1{k1}, xmm2, xmm3, 1	1	0.33
XED_IFORM_VPTERNLOGQ_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vpternlogq ymm1{k1}, ymm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGQ_YMMu64_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vpternlogq ymm1{k1}, ymm2, ymm3, 1	1	0.33
XED_IFORM_VPTERNLOGQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vpternlogq zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vpternlogq zmm1{k1}, zmm2, zmm3, 1	1	0.5
XED_IFORM_PTEST_XMMdq_MEMdq	vptest xmm1, [rdi]	9	1
XED_IFORM_VPTEST_XMMdq_MEMdq	vptest xmm1, [rdi]	9	1
XED_IFORM_PTEST_XMMdq_XMMdq	vptest xmm1, xmm2	3	1
XED_IFORM_VPTEST_XMMdq_XMMdq	vptest xmm1, xmm2	3	1
XED_IFORM_VPTEST_YMMqq_MEMqq	vptest ymm1, [rdi]	10	1
XED_IFORM_VPTEST_YMMqq_YMMqq	vptest ymm1, ymm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vptestmb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vptestmb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vptestmb k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vptestmb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vptestmb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vptestmb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_XMMu32_MEMu32_AVX512	vptestmd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_XMMu32_XMMu32_AVX512	vptestmd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_YMMu32_MEMu32_AVX512	vptestmd k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_YMMu32_YMMu32_AVX512	vptestmd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_ZMMu32_MEMu32_AVX512	vptestmd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_AVX512	vptestmd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_XMMu64_MEMu64_AVX512	vptestmq k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_XMMu64_XMMu64_AVX512	vptestmq k1{k1}, xmm1, xmm2	3	1

XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_YMMu64_MEMu64_AVX512	vptestmq k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_YMMu64_YMMu64_AVX512	vptestmq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_AVX512	vptestmq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_AVX512	vptestmq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vptestmw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vptestmw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vptestmw k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vptestmw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vptestmw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vptestmw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vptestnmb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vptestnmb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vptestnmb k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vptestnmb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vptestnmb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vptestnmb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_XMMu32_MEMu32_AVX512	vptestnmd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_XMMu32_XMMu32_AVX512	vptestnmd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_YMMu32_MEMu32_AVX512	vptestnmd k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_YMMu32_YMMu32_AVX512	vptestnmd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_ZMMu32_MEMu32_AVX512	vptestnmd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_AVX512	vptestnmd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_XMMu64_MEMu64_AVX512	vptestnmq k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_XMMu64_XMMu64_AVX512	vptestnmq k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_YMMu64_MEMu64_AVX512	vptestnmq k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_YMMu64_YMMu64_AVX512	vptestnmq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_AVX512	vptestnmq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_AVX512	vptestnmq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vptestnmw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vptestnmw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vptestnmw k1{k1}, ymm1, [rdi]	10	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vptestnmw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vptestnmw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vptestnmw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PUNPCKHBW_XMMdq_MEMdq	vpunpckhbw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHBW_XMMdq_XMMq	vpunpckhbw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHBW_XMMdq_XMMdq_MEMdq	vpunpckhbw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHBW_XMMdq_XMMdq_XMMdq	vpunpckhbw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHBW_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpunpckhbw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHBW_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpunpckhbw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHBW_YMMqq_YMMqq_MEMqq	vpunpckhbw ymm1, ymm2, [rdi]	8	1

XED_IFORM_VPUNPCKHBW_YMMqq_YMMqq_YMMqq	vpunpckhbw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHBW_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpunpckhbw ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHBW_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpunpckhbw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHBW_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpunpckhbw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHBW_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpunpckhbw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHDQ_XMMdq_MEMdq	vpunpckhdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHDQ_XMMdq_XMMq	vpunpckhdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHDQ_XMMdq_XMMdq_MEMdq	vpunpckhdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHDQ_XMMdq_XMMdq_XMMdq	vpunpckhdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHDQ_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpunpckhdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHDQ_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpunpckhdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHDQ_YMMqq_YMMqq_MEMqq	vpunpckhdq ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHDQ_YMMqq_YMMqq_YMMqq	vpunpckhdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHDQ_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpunpckhdq ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHDQ_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpunpckhdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHDQ_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpunpckhdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHDQ_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpunpckhdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHQDQ_XMMdq_MEMdq	vpunpckhqdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHQDQ_XMMdq_XMMq	vpunpckhqdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHQDQ_XMMdq_XMMdq_MEMdq	vpunpckhqdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHQDQ_XMMdq_XMMdq_XMMdq	vpunpckhqdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHQDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpunpckhqdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHQDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpunpckhqdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHQDQ_YMMqq_YMMqq_MEMqq	vpunpckhqdq ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHQDQ_YMMqq_YMMqq_YMMqq	vpunpckhqdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHQDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpunpckhqdq ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHQDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpunpckhqdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHQDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpunpckhqdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHQDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpunpckhqdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHWD_XMMdq_MEMdq	vpunpckhwd xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHWD_XMMdq_XMMq	vpunpckhwd xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHWD_XMMdq_XMMdq_MEMdq	vpunpckhwd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHWD_XMMdq_XMMdq_XMMdq	vpunpckhwd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHWD_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpunpckhwd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHWD_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpunpckhwd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHWD_YMMqq_YMMqq_MEMqq	vpunpckhwd ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHWD_YMMqq_YMMqq_YMMqq	vpunpckhwd ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHWD_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpunpckhwd ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKHWD_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpunpckhwd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHWD_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpunpckhwd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHWD_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpunpckhwd zmm1{k1}, zmm2, zmm3	1	1

XED_IFORM_PUNPCKLBW_XMMdq_MEMdq	vpunpcklbw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLBW_XMMdq_XMMq	vpunpcklbw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLBW_XMMdq_XMMdq_MEMdq	vpunpcklbw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLBW_XMMdq_XMMdq_XMMdq	vpunpcklbw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLBW_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpunpcklbw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLBW_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpunpcklbw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLBW_YMMqq_YMMqq_MEMqq	vpunpcklbw ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLBW_YMMqq_YMMqq_YMMqq	vpunpcklbw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLBW_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpunpcklbw ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLBW_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpunpcklbw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLBW_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpunpcklbw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLBW_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpunpcklbw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLDQ_XMMdq_MEMdq	vpunpckldq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLDQ_XMMdq_XMMq	vpunpckldq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLDQ_XMMdq_XMMdq_MEMdq	vpunpckldq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLDQ_XMMdq_XMMdq_XMMdq	vpunpckldq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLDQ_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpunpckldq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLDQ_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpunpckldq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLDQ_YMMqq_YMMqq_MEMqq	vpunpckldq ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLDQ_YMMqq_YMMqq_YMMqq	vpunpckldq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLDQ_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpunpckldq ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLDQ_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpunpckldq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLDQ_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpunpckldq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLDQ_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpunpckldq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLQDQ_XMMdq_MEMdq	vpunpcklqdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLQDQ_XMMdq_XMMq	vpunpcklqdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLQDQ_XMMdq_XMMdq_MEMdq	vpunpcklqdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLQDQ_XMMdq_XMMdq_XMMdq	vpunpcklqdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLQDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpunpcklqdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLQDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpunpcklqdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLQDQ_YMMqq_YMMqq_MEMqq	vpunpcklqdq ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLQDQ_YMMqq_YMMqq_YMMqq	vpunpcklqdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLQDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpunpcklqdq ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLQDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpunpcklqdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLQDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpunpcklqdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLQDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpunpcklqdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLWD_XMMdq_MEMdq	vpunpcklwd xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLWD_XMMdq_XMMq	vpunpcklwd xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLWD_XMMdq_XMMdq_MEMdq	vpunpcklwd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLWD_XMMdq_XMMdq_XMMdq	vpunpcklwd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLWD_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpunpcklwd xmm1{k1}, xmm2, [rdi]	7	1

XED_IFORM_VPUNPCKLWD_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpunpcklwd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLWD_YMMqq_YMMqq_MEMqq	vpunpcklwd ymm1, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLWD_YMMqq_YMMqq_YMMqq	vpunpcklwd ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLWD_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpunpcklwd ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VPUNPCKLWD_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpunpcklwd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLWD_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpunpcklwd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLWD_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpunpcklwd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PXOR_XMMdq_MEMdq	vpxor xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PXOR_XMMdq_XMMdq	vpxor xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPXOR_XMMdq_XMMdq_MEMdq	vpxor xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPXOR_XMMdq_XMMdq_XMMdq	vpxor xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPXOR_YMMqq_YMMqq_MEMqq	vpxor ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VPXOR_YMMqq_YMMqq_YMMqq	vpxor ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPXORD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpxord xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPXORD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpxord xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPXORD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpxord ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPXORD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpxord ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPXORD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpxord zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPXORD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpxord zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPXORQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpxorq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPXORQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpxorq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPXORQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpxorq ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VPXORQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpxorq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPXORQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpxorq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPXORQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpxorq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VRANGEPD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrangepd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGEPD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrangepd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGEPD_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vrangepd ymm1{k1}, ymm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPD_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vrangepd ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VRANGEPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vrangepd zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vrangepd zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VRANGEPS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrangeps xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGEPS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrangeps xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGEPS_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vrangeps ymm1{k1}, ymm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPS_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vrangeps ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VRANGEPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vrangeps zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vrangeps zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VRANGESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrangesd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrangesd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrangess xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrangess xmm1{k1}, xmm2, xmm3, 1	4	0.5

XED_IFORM_VRCP14PD_XMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd xmm1{k1}, [rdi]	10	1
XED_IFORM_VRCP14PD_XMMf64_MASKmskw_XMMf64_AVX512	vrcp14pd xmm1{k1}, xmm2	4	1
XED_IFORM_VRCP14PD_YMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd ymm1{k1}, [rdi]	11	1
XED_IFORM_VRCP14PD_YMMf64_MASKmskw_YMMf64_AVX512	vrcp14pd ymm1{k1}, ymm2	4	1
XED_IFORM_VRCP14PD_ZMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd zmm1{k1}, [rdi]	16	2
XED_IFORM_VRCP14PD_ZMMf64_MASKmskw_ZMMf64_AVX512	vrcp14pd zmm1{k1}, zmm2	9	2
XED_IFORM_VRCP14PS_XMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps xmm1{k1}, [rdi]	10	1
XED_IFORM_VRCP14PS_XMMf32_MASKmskw_XMMf32_AVX512	vrcp14ps xmm1{k1}, xmm2	4	1
XED_IFORM_VRCP14PS_YMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps ymm1{k1}, [rdi]	11	1
XED_IFORM_VRCP14PS_YMMf32_MASKmskw_YMMf32_AVX512	vrcp14ps ymm1{k1}, ymm2	4	1
XED_IFORM_VRCP14PS_ZMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps zmm1{k1}, [rdi]	16	2
XED_IFORM_VRCP14PS_ZMMf32_MASKmskw_ZMMf32_AVX512	vrcp14ps zmm1{k1}, zmm2	9	2
XED_IFORM_VRCP14SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vrcp14sd xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRCP14SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vrcp14sd xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_VRCP14SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vrcp14ss xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRCP14SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vrcp14ss xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_RCPPS_XMMps_MEMps	vrcpps xmm1, [rdi]	10	1
XED_IFORM_VRCPPS_XMMdq_MEMdq	vrcpps xmm1, [rdi]	10	1
XED_IFORM_VRCPPS_XMMdq_XMMdq	vrcpps xmm1, xmm2	4	1
XED_IFORM_RCPPS_XMMps_XMMps	vrcpps xmm1, xmm2	4	1
XED_IFORM_VRCPPS_YMMqq_MEMqq	vrcpps ymm1, [rdi]	11	1
XED_IFORM_VRCPPS_YMMqq_YMMqq	vrcpps ymm1, ymm2	4	1
XED_IFORM_RCPSS_XMMss_MEMss	vrcpss xmm1, xmm1, [rdi]	9	1
XED_IFORM_RCPSS_XMMss_XMMss	vrcpss xmm1, xmm1, xmm2	4	1
XED_IFORM_VRCPSS_XMMdq_XMMdq_MEMd	vrcpss xmm1, xmm2, [rdi]	9	1
XED_IFORM_VRCPSS_XMMdq_XMMdq_XMMd	vrcpss xmm1, xmm2, xmm3	4	1
XED_IFORM_VREDUCEPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VREDUCEPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vreducepd xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VREDUCEPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd ymm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vreducepd ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VREDUCEPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd zmm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vreducepd zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VREDUCEPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VREDUCEPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vreduceps xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VREDUCEPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps ymm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vreduceps ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VREDUCEPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps zmm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vreduceps zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VREDUCESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vreducesd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VREDUCESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vreducesd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VREDUCESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vreducess xmm1{k1}, xmm2, [rdi], 1	10	0.5

XED_IFORM_VREDUCESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vreducess xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRNDSCALEPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd xmm1{k1}, [rdi], 1	14	1
XED_IFORM_VRNDSCALEPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vrndscalepd xmm1{k1}, xmm2, 1	8	1
XED_IFORM_VRNDSCALEPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd ymm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vrndscalepd ymm1{k1}, ymm2, 1	8	1
XED_IFORM_VRNDSCALEPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd zmm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vrndscalepd zmm1{k1}, zmm2, 1	8	1
XED_IFORM_VRNDSCALEPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps xmm1{k1}, [rdi], 1	14	1
XED_IFORM_VRNDSCALEPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vrndscaleps xmm1{k1}, xmm2, 1	8	1
XED_IFORM_VRNDSCALEPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps ymm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vrndscaleps ymm1{k1}, ymm2, 1	8	1
XED_IFORM_VRNDSCALEPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps zmm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vrndscaleps zmm1{k1}, zmm2, 1	8	1
XED_IFORM_VRNDSCALESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrndscalesd xmm1{k1}, xmm2, [rdi], 1	14	1
XED_IFORM_VRNDSCALESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrndscalesd xmm1{k1}, xmm2, xmm3, 1	8	1
XED_IFORM_VRNDSCALESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrndscaless xmm1{k1}, xmm2, [rdi], 1	14	1
XED_IFORM_VRNDSCALESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrndscaless xmm1{k1}, xmm2, xmm3, 1	8	1
XED_IFORM_ROUNDPD_XMMpd_MEMpd_IMMb	vroundpd xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPD_XMMdq_MEMdq_IMMb	vroundpd xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPD_XMMdq_XMMdq_IMMb	vroundpd xmm1, xmm2, 1	8	1
XED_IFORM_ROUNDPD_XMMpd_XMMpd_IMMb	vroundpd xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDPD_YMMqq_MEMqq_IMMb	vroundpd ymm1, [rdi], 1	15	1
XED_IFORM_VROUNDPD_YMMqq_YMMqq_IMMb	vroundpd ymm1, ymm2, 1	8	1
XED_IFORM_VROUNDPS_XMMdq_MEMdq_IMMb	vroundps xmm1, [rdi], 1	14	1
XED_IFORM_ROUNDPS_XMMps_MEMps_IMMb	vroundps xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPS_XMMdq_XMMdq_IMMb	vroundps xmm1, xmm2, 1	8	1
XED_IFORM_ROUNDPS_XMMps_XMMps_IMMb	vroundps xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDPS_YMMqq_MEMqq_IMMb	vroundps ymm1, [rdi], 1	15	1
XED_IFORM_VROUNDPS_YMMqq_YMMqq_IMMb	vroundps ymm1, ymm2, 1	8	1
XED_IFORM_ROUNDSD_XMMq_MEMq_IMMb	vroundsd xmm1, xmm1, [rdi], 1	14	1
XED_IFORM_ROUNDSD_XMMq_XMMq_IMMb	vroundsd xmm1, xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDSD_XMMdq_XMMdq_MEMq_IMMb	vroundsd xmm1, xmm2, [rdi], 1	14	1
XED_IFORM_VROUNDSD_XMMdq_XMMdq_XMMq_IMMb	vroundsd xmm1, xmm2, xmm3, 1	8	1
XED_IFORM_ROUNDSS_XMMd_MEMd_IMMb	vroundss xmm1, xmm1, [rdi], 1	14	1
XED_IFORM_ROUNDSS_XMMd_XMMd_IMMb	vroundss xmm1, xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDSS_XMMdq_XMMdq_MEMd_IMMb	vroundss xmm1, xmm2, [rdi], 1	14	1
XED_IFORM_VROUNDSS_XMMdq_XMMdq_XMMd_IMMb	vroundss xmm1, xmm2, xmm3, 1	8	1
XED_IFORM_VRSQRT14PD_XMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd xmm1{k1}, [rdi]	10	1
XED_IFORM_VRSQRT14PD_XMMf64_MASKmskw_XMMf64_AVX512	vrsqrt14pd xmm1{k1}, xmm2	4	1
XED_IFORM_VRSQRT14PD_YMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd ymm1{k1}, [rdi]	11	1
XED_IFORM_VRSQRT14PD_YMMf64_MASKmskw_YMMf64_AVX512	vrsqrt14pd ymm1{k1}, ymm2	4	1

XED_IFORM_VRSQRT14PD_ZMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd zmm1{k1}, [rdi]	16	2
XED_IFORM_VRSQRT14PD_ZMMf64_MASKmskw_ZMMf64_AVX512	vrsqrt14pd zmm1{k1}, zmm2	9	2
XED_IFORM_VRSQRT14PS_XMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps xmm1{k1}, [rdi]	10	1
XED_IFORM_VRSQRT14PS_XMMf32_MASKmskw_XMMf32_AVX512	vrsqrt14ps xmm1{k1}, xmm2	4	1
XED_IFORM_VRSQRT14PS_YMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps ymm1{k1}, [rdi]	11	1
XED_IFORM_VRSQRT14PS_YMMf32_MASKmskw_YMMf32_AVX512	vrsqrt14ps ymm1{k1}, ymm2	4	1
XED_IFORM_VRSQRT14PS_ZMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps zmm1{k1}, [rdi]	16	2
XED_IFORM_VRSQRT14PS_ZMMf32_MASKmskw_ZMMf32_AVX512	vrsqrt14ps zmm1{k1}, zmm2	9	2
XED_IFORM_VRSQRT14SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vrsqrt14sd xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRSQRT14SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vrsqrt14sd xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_VRSQRT14SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vrsqrt14ss xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRSQRT14SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vrsqrt14ss xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_VRSQRTPS_XMMdq_MEMdq	vrsqrtps xmm1, [rdi]	10	1
XED_IFORM_RSQRTPS_XMMps_MEMps	vrsqrtps xmm1, [rdi]	10	1
XED_IFORM_VRSQRTPS_XMMdq_XMMdq	vrsqrtps xmm1, xmm2	4	1
XED_IFORM_RSQRTPS_XMMps_XMMps	vrsqrtps xmm1, xmm2	4	1
XED_IFORM_VRSQRTPS_YMMqq_MEMqq	vrsqrtps ymm1, [rdi]	11	1
XED_IFORM_VRSQRTPS_YMMqq_YMMqq	vrsqrtps ymm1, ymm2	4	1
XED_IFORM_RSQRTSS_XMMss_MEMss	vrsqrtss xmm1, xmm1, [rdi]	9	1
XED_IFORM_RSQRTSS_XMMss_XMMss	vrsqrtss xmm1, xmm1, xmm2	4	1
XED_IFORM_VRSQRTSS_XMMdq_XMMdq_MEMd	vrsqrtss xmm1, xmm2, [rdi]	9	1
XED_IFORM_VRSQRTSS_XMMdq_XMMdq_XMMd	vrsqrtss xmm1, xmm2, xmm3	4	1
XED_IFORM_VSCALEFPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vscalefpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vscalefpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vscalefpd ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vscalefpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSCALEFPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vscalefpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vscalefpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VSCALEFPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vscalefps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vscalefps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vscalefps ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vscalefps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSCALEFPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vscalefps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vscalefps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VSCALEFSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vscalefsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vscalefsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vscalefss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vscalefss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_XMMf64_AVX512_VL128	vscatterdpd [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_YMMf64_AVX512_VL256	vscatterdpd [rdi+xmm1*1]{k1}, ymm2	11	4
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_ZMMf64_AVX512_VL512	vscatterdpd [rdi+ymm1*1]{k1}, zmm2	11	8

XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_XMMf32_AVX512_VL128	vscatterdps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_YMMf32_AVX512_VL256	vscatterdps [rdi+ymm1*1]{k1}, ymm2	12	8
XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_ZMMf32_AVX512_VL512	vscatterdps [rdi+zmm1*1]{k1}, zmm2	11	16.75
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_XMMf64_AVX512_VL128	vscatterqpd [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_YMMf64_AVX512_VL256	vscatterqpd [rdi+ymm1*1]{k1}, ymm2	11	4
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_ZMMf64_AVX512_VL512	vscatterqpd [rdi+zmm1*1]{k1}, zmm2	11	8
XED_IFORM_VSCATTERQPS_MEMf32_MASKmskw_XMMf32_AVX512_VL128	vscatterqps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSCATTERQPS_MEMf32_MASKmskw_XMMf32_AVX512_VL256	vscatterqps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSHUFF32X4_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vshuff32x4 ymm1{k1}, ymm2, [rdi], 1	10	1
XED_IFORM_VSHUFF32X4_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vshuff32x4 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFF32X4_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vshuff32x4 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFF32X4_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vshuff32x4 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFF64X2_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vshuff64x2 ymm1{k1}, ymm2, [rdi], 1	10	1
XED_IFORM_VSHUFF64X2_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vshuff64x2 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFF64X2_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vshuff64x2 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFF64X2_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vshuff64x2 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFI32X4_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vshufi32x4 ymm1{k1}, ymm2, [rdi], 1	10	1
XED_IFORM_VSHUFI32X4_YMMu32_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vshufi32x4 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFI32X4_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vshufi32x4 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFI32X4_ZMMu32_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vshufi32x4 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFI64X2_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vshufi64x2 ymm1{k1}, ymm2, [rdi], 1	10	1
XED_IFORM_VSHUFI64X2_YMMu64_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vshufi64x2 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFI64X2_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vshufi64x2 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFI64X2_ZMMu64_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vshufi64x2 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_SHUFPD_XMMpd_MEMpd_IMMb	vshufpd xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_SHUFPD_XMMpd_XMMpd_IMMb	vshufpd xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VSHUFPD_XMMdq_XMMdq_MEMdq_IMMb	vshufpd xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPD_XMMdq_XMMdq_XMMdq_IMMb	vshufpd xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vshufpd xmm1{k1}, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vshufpd xmm1{k1}, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPD_YMMqq_YMMqq_MEMqq_IMMb	vshufpd ymm1, ymm2, [rdi], 1	8	1
XED_IFORM_VSHUFPD_YMMqq_YMMqq_YMMqq_IMMb	vshufpd ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPD_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vshufpd ymm1{k1}, ymm2, [rdi], 1	8	1
XED_IFORM_VSHUFPD_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vshufpd ymm1{k1}, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vshufpd zmm1{k1}, zmm2, [rdi], 1	8	1
XED_IFORM_VSHUFPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vshufpd zmm1{k1}, zmm2, zmm3, 1	1	1
XED_IFORM_SHUFPS_XMMps_MEMps_IMMb	vshufps xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_SHUFPS_XMMps_XMMps_IMMb	vshufps xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VSHUFPS_XMMdq_XMMdq_MEMdq_IMMb	vshufps xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPS_XMMdq_XMMdq_XMMdq_IMMb	vshufps xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vshufps xmm1{k1}, xmm2, [rdi], 1	7	1

XED_IFORM_VSHUFPS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vshufps xmm1{k1}, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPS_YMMqq_YMMqq_MEMqq_IMMb	vshufps ymm1, ymm2, [rdi], 1	8	1
XED_IFORM_VSHUFPS_YMMqq_YMMqq_YMMqq_IMMb	vshufps ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPS_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vshufps ymm1{k1}, ymm2, [rdi], 1	8	1
XED_IFORM_VSHUFPS_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vshufps ymm1{k1}, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vshufps zmm1{k1}, zmm2, [rdi], 1	8	1
XED_IFORM_VSHUFPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vshufps zmm1{k1}, zmm2, zmm3, 1	1	1
XED_IFORM_SQRTPD_XMMpd_MEMpd	vsqrtpd xmm1, [rdi]	24	6
XED_IFORM_VSQRTPD_XMMdq_MEMdq	vsqrtpd xmm1, [rdi]	24	6
XED_IFORM_SQRTPD_XMMpd_XMMpd	vsqrtpd xmm1, xmm2	18	6
XED_IFORM_VSQRTPD_XMMdq_XMMdq	vsqrtpd xmm1, xmm2	18	6
XED_IFORM_VSQRTPD_XMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd xmm1{k1}, [rdi]	24	6
XED_IFORM_VSQRTPD_XMMf64_MASKmskw_XMMf64_AVX512	vsqrtpd xmm1{k1}, xmm2	18	6
XED_IFORM_VSQRTPD_YMMqq_MEMqq	vsqrtpd ymm1, [rdi]	25	12
XED_IFORM_VSQRTPD_YMMqq_YMMqq	vsqrtpd ymm1, ymm2	18	12
XED_IFORM_VSQRTPD_YMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd ymm1{k1}, [rdi]	25	12
XED_IFORM_VSQRTPD_YMMf64_MASKmskw_YMMf64_AVX512	vsqrtpd ymm1{k1}, ymm2	18	12
XED_IFORM_VSQRTPD_ZMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd zmm1{k1}, [rdi]	38	24
XED_IFORM_VSQRTPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vsqrtpd zmm1{k1}, zmm2	31	24
XED_IFORM_VSQRTPS_XMMdq_MEMdq	vsqrtps xmm1, [rdi]	18	3
XED_IFORM_SQRTPS_XMMps_MEMps	vsqrtps xmm1, [rdi]	18	3
XED_IFORM_VSQRTPS_XMMdq_XMMdq	vsqrtps xmm1, xmm2	12	3
XED_IFORM_SQRTPS_XMMps_XMMps	vsqrtps xmm1, xmm2	12	3
XED_IFORM_VSQRTPS_XMMf32_MASKmskw_MEMf32_AVX512	vsqrtps xmm1{k1}, [rdi]	18	3
XED_IFORM_VSQRTPS_XMMf32_MASKmskw_XMMf32_AVX512	vsqrtps xmm1{k1}, xmm2	12	3
XED_IFORM_VSQRTPS_YMMqq_MEMqq	vsqrtps ymm1, [rdi]	19	6
XED_IFORM_VSQRTPS_YMMqq_YMMqq	vsqrtps ymm1, ymm2	12	6
XED_IFORM_VSQRTPS_YMMf32_MASKmskw_MEMf32_AVX512	vsqrtps ymm1{k1}, [rdi]	19	6
XED_IFORM_VSQRTPS_YMMf32_MASKmskw_YMMf32_AVX512	vsqrtps ymm1{k1}, ymm2	12	6
XED_IFORM_VSQRTPS_ZMMf32_MASKmskw_MEMf32_AVX512	vsqrtps zmm1{k1}, [rdi]	26	12
XED_IFORM_VSQRTPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vsqrtps zmm1{k1}, zmm2	19	12
XED_IFORM_SQRTSD_XMMsd_MEMsd	vsqrtsd xmm1, xmm1, [rdi]	23	6
XED_IFORM_SQRTSD_XMMsd_XMMsd	vsqrtsd xmm1, xmm1, xmm2	18	6
XED_IFORM_VSQRTSD_XMMdq_XMMdq_MEMq	vsqrtsd xmm1, xmm2, [rdi]	23	6
XED_IFORM_VSQRTSD_XMMdq_XMMdq_XMMq	vsqrtsd xmm1, xmm2, xmm3	18	6
XED_IFORM_VSQRTSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsqrtsd xmm1{k1}, xmm2, [rdi]	24	6
XED_IFORM_VSQRTSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsqrtsd xmm1{k1}, xmm2, xmm3	18	6
XED_IFORM_SQRTSS_XMMss_MEMss	vsqrtss xmm1, xmm1, [rdi]	17	3
XED_IFORM_SQRTSS_XMMss_XMMss	vsqrtss xmm1, xmm1, xmm2	12	3
XED_IFORM_VSQRTSS_XMMdq_XMMdq_MEMd	vsqrtss xmm1, xmm2, [rdi]	17	3
XED_IFORM_VSQRTSS_XMMdq_XMMdq_XMMd	vsqrtss xmm1, xmm2, xmm3	12	3

XED_IFORM_VSQRTSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsqrtss xmm1{k1}, xmm2, [rdi]	18	3
XED_IFORM_VSQRTSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsqrtss xmm1{k1}, xmm2, xmm3	12	3
XED_IFORM_STMXCSR_MEMd	vstmxcsr [rdi]	6	1
XED_IFORM_VSTMXCSR_MEMd	vstmxcsr [rdi]	6	1
XED_IFORM_SUBPD_XMMpd_MEMpd	vsubpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_SUBPD_XMMpd_XMMpd	vsubpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBPD_XMMdq_XMMdq_MEMdq	vsubpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPD_XMMdq_XMMdq_XMMdq	vsubpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsubpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsubpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPD_YMMqq_YMMqq_MEMqq	vsubpd ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VSUBPD_YMMqq_YMMqq_YMMqq	vsubpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vsubpd ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VSUBPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vsubpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vsubpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSUBPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vsubpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_SUBPS_XMMps_MEMps	vsubps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_SUBPS_XMMps_XMMps	vsubps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBPS_XMMdq_XMMdq_MEMdq	vsubps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPS_XMMdq_XMMdq_XMMdq	vsubps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsubps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsubps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPS_YMMqq_YMMqq_MEMqq	vsubps ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VSUBPS_YMMqq_YMMqq_YMMqq	vsubps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vsubps ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VSUBPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vsubps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vsubps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSUBPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vsubps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_SUBSD_XMMsd_MEMsd	vsubsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_SUBSD_XMMsd_XMMsd	vsubsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBSD_XMMdq_XMMdq_MEMq	vsubsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VSUBSD_XMMdq_XMMdq_XMMq	vsubsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsubsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsubsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_SUBSS_XMMss_MEMss	vsubss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_SUBSS_XMMss_XMMss	vsubss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBSS_XMMdq_XMMdq_MEMd	vsubss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VSUBSS_XMMdq_XMMdq_XMMd	vsubss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsubss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsubss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VTESTPD_XMMdq_MEMdq	vtestpd xmm1, [rdi]	8	1

XED_IFORM_VTESTPD_XMMdq_XMMdq	vtestpd xmm1, xmm2	2	1
XED_IFORM_VTESTPD_YMMqq_MEMqq	vtestpd ymm1, [rdi]	9	1
XED_IFORM_VTESTPD_YMMqq_YMMqq	vtestpd ymm1, ymm2	2	1
XED_IFORM_VTESTPS_XMMdq_MEMdq	vtestps xmm1, [rdi]	8	1
XED_IFORM_VTESTPS_XMMdq_XMMdq	vtestps xmm1, xmm2	2	1
XED_IFORM_VTESTPS_YMMqq_MEMqq	vtestps ymm1, [rdi]	9	1
XED_IFORM_VTESTPS_YMMqq_YMMqq	vtestps ymm1, ymm2	2	1
XED_IFORM_VUCOMISD_XMMf64_MEMf64_AVX512	vucomisd xmm1, [rdi]	8	1
XED_IFORM_VUCOMISD_XMMdq_MEMq	vucomisd xmm1, [rdi]	8	1
XED_IFORM_UCOMISD_XMMsd_MEMsd	vucomisd xmm1, [rdi]	8	1
XED_IFORM_UCOMISD_XMMsd_XMMsd	vucomisd xmm1, xmm2	3	1
XED_IFORM_VUCOMISD_XMMdq_XMMq	vucomisd xmm1, xmm2	3	1
XED_IFORM_VUCOMISD_XMMf64_XMMf64_AVX512	vucomisd xmm1, xmm2	3	1
XED_IFORM_VUCOMISS_XMMf32_MEMf32_AVX512	vucomiss xmm1, [rdi]	8	1
XED_IFORM_VUCOMISS_XMMdq_MEMd	vucomiss xmm1, [rdi]	8	1
XED_IFORM_UCOMISS_XMMss_MEMss	vucomiss xmm1, [rdi]	8	1
XED_IFORM_VUCOMISS_XMMf32_XMMf32_AVX512	vucomiss xmm1, xmm2	3	1
XED_IFORM_VUCOMISS_XMMdq_XMMd	vucomiss xmm1, xmm2	3	1
XED_IFORM_UCOMISS_XMMss_XMMss	vucomiss xmm1, xmm2	3	1
XED_IFORM_UNPCKHPD_XMMpd_MEMdq	vunpckhpd xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKHPD_XMMpd_XMMq	vunpckhpd xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKHPD_XMMdq_XMMdq_MEMdq	vunpckhpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPD_XMMdq_XMMdq_XMMdq	vunpckhpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vunpckhpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vunpckhpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPD_YMMqq_YMMqq_MEMqq	vunpckhpd ymm1, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKHPD_YMMqq_YMMqq_YMMqq	vunpckhpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vunpckhpd ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKHPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vunpckhpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vunpckhpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKHPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vunpckhpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKHPS_XMMps_MEMdq	vunpckhps xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKHPS_XMMps_XMMdq	vunpckhps xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKHPS_XMMdq_XMMdq_MEMdq	vunpckhps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPS_XMMdq_XMMdq_XMMdq	vunpckhps xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vunpckhps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vunpckhps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPS_YMMqq_YMMqq_MEMqq	vunpckhps ymm1, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKHPS_YMMqq_YMMqq_YMMqq	vunpckhps ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vunpckhps ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKHPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vunpckhps ymm1{k1}, ymm2, ymm3	1	1

XED_IFORM_VUNPCKHPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vunpckhps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKHPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vunpckhps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKLPD_XMMpd_MEMdq	vunpcklpd xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKLPD_XMMpd_XMMq	vunpcklpd xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKLPD_XMMdq_XMMdq_MEMdq	vunpcklpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPD_XMMdq_XMMdq_XMMdq	vunpcklpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vunpcklpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vunpcklpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPD_YMMqq_YMMqq_MEMqq	vunpcklpd ymm1, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKLPD_YMMqq_YMMqq_YMMqq	vunpcklpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vunpcklpd ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKLPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vunpcklpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vunpcklpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKLPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vunpcklpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKLPS_XMMps_MEMdq	vunpcklps xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKLPS_XMMps_XMMq	vunpcklps xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKLPS_XMMdq_XMMdq_MEMdq	vunpcklps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPS_XMMdq_XMMdq_XMMdq	vunpcklps xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vunpcklps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vunpcklps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPS_YMMqq_YMMqq_MEMqq	vunpcklps ymm1, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKLPS_YMMqq_YMMqq_YMMqq	vunpcklps ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vunpcklps ymm1{k1}, ymm2, [rdi]	8	1
XED_IFORM_VUNPCKLPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vunpcklps ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vunpcklps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKLPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vunpcklps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_XORPD_XMMpd_MEMpd	vxorpd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_XORPD_XMMpd_XMMpd	vxorpd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VXORPD_XMMdq_XMMdq_MEMdq	vxorpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPD_XMMdq_XMMdq_XMMdq	vxorpd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VXORPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vxorpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vxorpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VXORPD_YMMqq_YMMqq_MEMqq	vxorpd ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VXORPD_YMMqq_YMMqq_YMMqq	vxorpd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VXORPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vxorpd ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VXORPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vxorpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VXORPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vxorpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VXORPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vxorpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_XORPS_XMMps_MEMps	vxorps xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_XORPS_XMMps_XMMps	vxorps xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VXORPS_XMMdq_XMMdq_MEMdq	vxorps xmm1, xmm2, [rdi]	7	0.5

XED_IFORM_VXORPS_XMMdq_XMMdq_XMMdq	vxorps xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VXORPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vxorps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vxorps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VXORPS_YMMqq_YMMqq_MEMqq	vxorps ymm1, ymm2, [rdi]	8	0.5
XED_IFORM_VXORPS_YMMqq_YMMqq_YMMqq	vxorps ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VXORPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vxorps ymm1{k1}, ymm2, [rdi]	8	0.5
XED_IFORM_VXORPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vxorps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VXORPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vxorps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VXORPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vxorps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VZEROALL	vzeroall	16	4
XED_IFORM_VZEROUPPER	vzeroupper	4	1
XED_IFORM_XADD_MEMb_GPR8	xadd [rdi], al	7	1
XED_IFORM_XADD_MEMv_GPRv	xadd [rdi], rax	7	1
XED_IFORM_XADD_GPR8_GPR8	xadd al, cl	3	0.75
XED_IFORM_XADD_GPRv_GPRv	xadd rax, rcx	3	0.75
XED_IFORM_XCHG_MEMb_GPR8	xchg [rdi], al	10	1.25
XED_IFORM_XCHG_MEMv_GPRv	xchg [rdi], rax	10	1.25
XED_IFORM_XCHG_GPR8_GPR8	xchg cl, al	3	0.75
XED_IFORM_XCHG_GPRv_GPRv	xchg rcx, rax	1	0.25
XED_IFORM_XGETBV	xgetbv	2	0.5
XED_IFORM_XOR_MEMv_IMMb	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMv_IMMz	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMb_IMMb_82r6	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMb_IMMb_80r6	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMb_GPR8	xor [rdi], al	6	1
XED_IFORM_XOR_MEMv_GPRv	xor [rdi], rax	6	1
XED_IFORM_XOR_GPR8_MEMb	xor al, [rdi]	6	0.5
XED_IFORM_XOR_AL_IMMb	xor al, 1	1	0.25
XED_IFORM_XOR_GPR8_IMMb_80r6	xor al, 1	1	0.25
XED_IFORM_XOR_GPR8_IMMb_82r6	xor al, 1	1	0.25
XED_IFORM_XOR_GPR8_GPR8_30	xor al, cl	0	0.25
XED_IFORM_XOR_GPR8_GPR8_32	xor al, cl	0	0.25
XED_IFORM_XOR_OrAX_IMMz	xor ax, 1	1	0.25
XED_IFORM_XOR_GPRv_MEMv	xor rax, [rdi]	6	0.5
XED_IFORM_XOR_GPRv_IMMz	xor rax, 1	1	0.25
XED_IFORM_XOR_GPRv_IMMb	xor rax, 1	1	0.25
XED_IFORM_XOR_GPRv_GPRv_31	xor rax, rcx	0	0.25
XED_IFORM_XOR_GPRv_GPRv_33	xor rax, rcx	0	0.25
XED_IFORM_XRSTOR_MEMmxsave	xrstor ptr [rdi]	37	8
XED_IFORM_XRSTOR64_MEMmxsave	xrstor64 ptr [rdi]	37	8
XED_IFORM_XSAVE_MEMmxsave	xsave ptr [rdi]	42	11

XED_IFORM_XSAVE64_MEMmxsave	xsave64 ptr [rdi]	41	10
XED_IFORM_XSAVEOPT_MEMmxsave	xsaveopt ptr [rdi]	46	11
XED_IFORM_XSAVEOPT64_MEMmxsave	xsaveopt64 ptr [rdi]	46	11
XED_IFORM_XSETBV	xsetbv	5	1.25

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