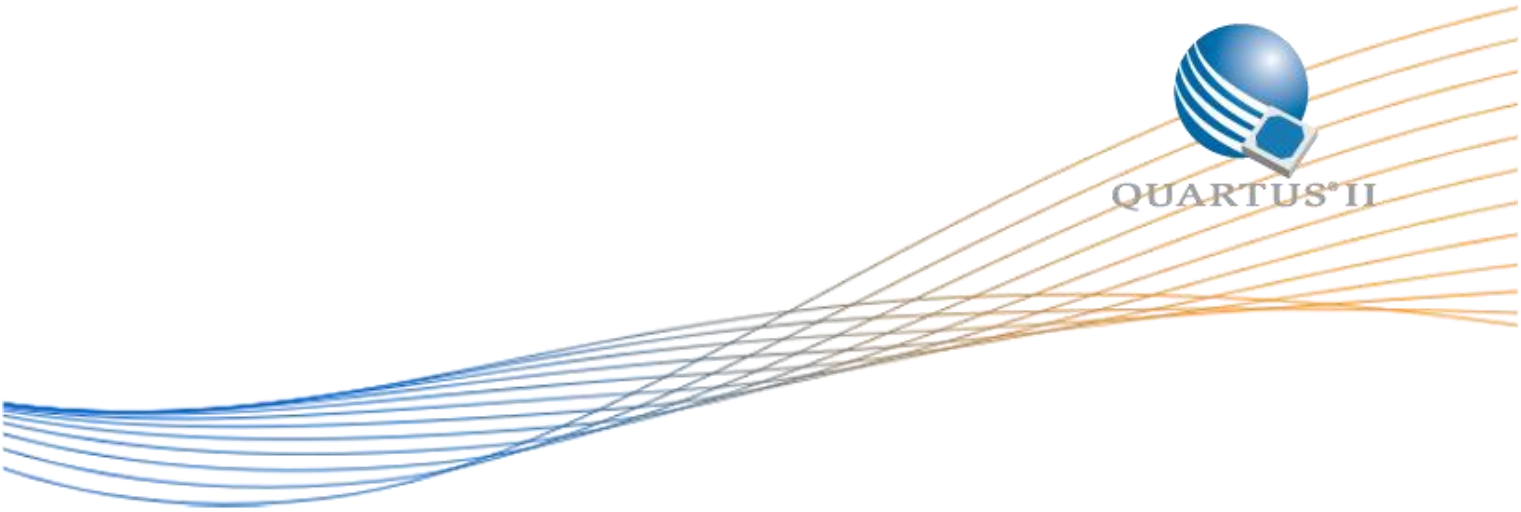

Arria 10 DDR3 x40 with EMIF Debug Toolkit

Date: 25 August 2015

Revision: 1.0

©2015 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

Table of Contents

List of Figure

List of Table

System Requirement

This example design targets the Arria 10 GX FPGA Development Kit. This design is a 40-bit wide, 1067-MHz DDR3 SDRAM interface working with a Arria 10 FPGA with External Memory Interface Toolkit.

The Arria 10 External Memory Interface IP also generates an example top level file, an example traffic generator, and a test bench including an external memory model. All these will be used to demonstrate the DDR3 SDRAM functionality.

Design Specifications

The design will utilize the HiLo External memory port on the Arria 10 GX Development Kit. We will be utilizing the DDR3 module that comes together with the development kit. The figure highlights those modules which we will be using on this design.

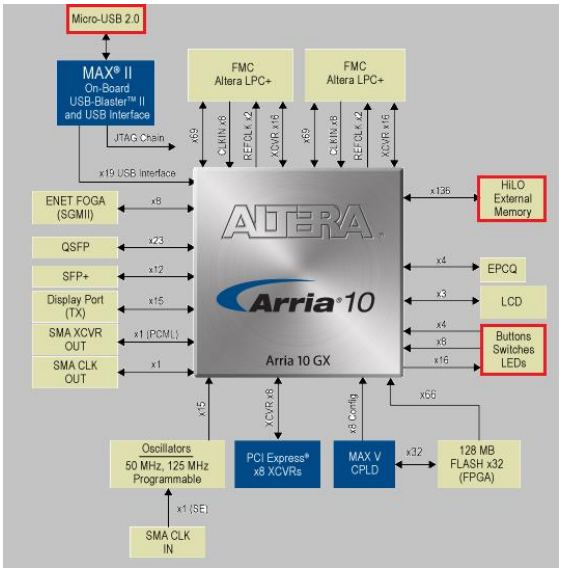

Figure 1: Arria 10 development kit connection used for DDR3 example design

The table below lists the specifications for this design:

Attribute	**Specification**
Quartus version	QuartusII v15.0
FPGA	10AX115S2F45I1SGE2
Kit	Developement Kit
Memory speed	1067MHz
Memory topology	x40-bit, 4 DDR3 SDRAM components
IP used	DDR3 SDRAM Arria 10 External Memory Interface IP and generated example top Quartus project

Table 1: Specification of design

Pin Assignment and Description

Pin	Location	I/O Standard	Description
dq[0]	B28	1.5V	DQ pin
dq[1]	A28	1.5V	DQ pin
dq[2]	A27	1.5V	DQ pin
dq[3]	B27	1.5V	DQ pin
dq[4]	D27	1.5V	DQ pin
dq[5]	E27	1.5V	DQ pin
dq[6]	D26	1.5V	DQ pin
dq[7]	D28	1.5V	DQ pin
dqs[0]	B26	1.5V	DQS pin
dqs_n[0]	C26	1.5V	DQS pin
dm[0]	E26	1.5V	DM pin
dq[8]	G25	1.5V	DQ pin
dq[9]	H25	1.5V	DQ pin
dq[10]	G26	1.5V	DQ pin
dq[11]	H26	1.5V	DQ pin
dq[12]	G28	1.5V	DQ pin
dq[13]	F27	1.5V	DQ pin
dq[14]	K27	1.5V	DQ pin
dq[15]	F28	1.5V	DQ pin
dqs[1]	H28	1.5V	DQS pin
dqs_n[1]	J27	1.5V	DQS pin
dm[1]	G27	1.5V	DM pin
dq[16]	D31	1.5V	DQ pin
dq[17]	E31	1.5V	DQ pin
dq[18]	B31	1.5V	DQ pin
dq[19]	C31	1.5V	DQ pin
dq[20]	A30	1.5V	DQ pin
dq[21]	E30	1.5V	DQ pin
dq[22]	B30	1.5V	DQ pin
dq[23]	D29	1.5V	DQ pin
dqs[2]	C30	1.5V	DQS pin
dqs_n[2]	C29	1.5V	DQS pin
dm[2]	A29	1.5V	DM pin

Table 2: Pin Assignment for Example Design

Pin	Location	I/O Standard	Description
dq[24]	K30	1.5V	DQ pin
dq[25]	H30	1.5V	DQ pin
dq[26]	G30	1.5V	DQ pin
dq[27]	K31	1.5V	DQ pin
dq[28]	H29	1.5V	DQ pin
dq[29]	K29	1.5V	DQ pin
dq[30]	J29	1.5V	DQ pin
dq[31]	F29	1.5V	DQ pin
dqs[3]	L30	1.5V	DQS pin
dqs_n[3]	L29	1.5V	DQS pin
dm[3]	F30	1.5V	DM pin
1dq[32]	AC3	1.5V	DQ pin
1dq[33]	AB3	1.5V	DQ pin
dq[34]	W31	1.5V	DQ pin
dq[35]	Y31	1.5V	DQ pin
dq[36]	AD31	1.5V	DQ pin
dq[37]	AD32	1.5V	DQ pin
dq[38]	AD33	1.5V	DQ pin
dq[39]	AA30	1.5V	DQ pin
dqs[4]	Y32	1.5V	DQS pin
2dqs_n[4]	AA3	1.5V	DQS pin
2dm[4]	AB3	1.5V	DM pin
rzqin	J34	1.5V	RZQ pin
a[0]	M32	1.5V	Address & Command pin
a[1]	L32	1.5V	Address & Command pin
a[2]	N34	1.5V	Address & Command pin
a[3]	M35	1.5V	Address & Command pin
a[4]	L34	1.5V	Address & Command pin
a[5]	K34	1.5V	Address & Command pin
a[6]	M33	1.5V	Address & Command pin
a[7]	L33	1.5V	Address & Command pin
a[8]	J33	1.5V	Address & Command pin
a[9]	J32	1.5V	Address & Command pin
a[10]	H31	1.5V	Address & Command pin
a[11]	J31	1.5V	Address & Command pin
a[12]	H34	1.5V	Address & Command pin
a[13]	H33	1.5V	Address & Command pin
a[14]	G32	1.5V	Address & Command pin

Table 3: Pin Assignment for Example Design

Pin	Location	I/O Standard	Description
ba[0]	F33	1.5V	Address & Command pin
ba[1]	G35	1.5V	Address & Command pin
ba[2]	H35	1.5V	Address & Command pin
cas_n[0]	G33	1.5V	Address & Command pin
ck[0]	R30	1.5V	Address & Command pin
ck_n[0]	R31	1.5V	Address & Command pin
cke[0]	U33	1.5V	Address & Command pin
cs_n[0]	R34	1.5V	Address & Command pin
odt[0]	N33	1.5V	Address & Command pin
ras_n[0]	F32	1.5V	Address & Command pin
reset_n[0]	T35	1.5V	Address & Command pin
we_n[0]	T34	1.5V	Address & Command pin
pll_ref_clk_clk(n)	F35	1.5V	pll reference clock pin
pll_ref_clk_clk	F34	1.5V	pll reference clock pin
status_local_cal_fail	L28	1.5V	status pin
status_local_cal_success	L27	1.5V	status pin
traffic_gen_fail	K25	1.5V	status pin
traffic_gen_pass	K24	1.5V	status pin
traffic_gen_timeout	J24	1.5V	status pin
global_reset_n	U11	1.5V	global reset pin

Table 4: Pin Assignment for Example Design

Design Hardwere Test

1. In the Quartus II software, launch **In-System Sources and Probes Editor** from **Tools** menu.
2. In **Jtag Chain Configuration** window under **In-System Sources and Probes Editor** GUI, configure the **Hardware** and **Device** based on the targeted board. For **File**, browse for the ed_synth.sof file and click **Open**.
3. Click **Program Device** button to configure the FPGA.
4. Once the configuration is successful (Ready to acquire), launch **SignalTap II Logic Analyzer** from **Tools** menu.
5. Select the SignalTap instance and click the **Autorun Analysis** button next to **Instance Manager** label. The SignalTap II Logic Analyzer Pane will shows the acquired data from each signal in the **Data** tab. At this stage, all signal will be low as the global_reset_n signal is still asserted.
6. In In-System Sources and Probes Editor Pane, click the **source[0]** instance value under the **Data** column to change it from 0 to 1. This will de-assert the global_reset_n signal in the hardware.
7. Now observe the data for **local_cal_success** and **traffic_gen_pass** and **traffice_gen_timeout** instances change from 0 to 1 on the SignalTap which indicate the calibration is success and pass the example driver tests.

External Memory Interface Toolkit Test

1. To understand the calibration value of the design you can use the **External Memory Interface Toolkit** from **Tools>System Debugging Tools** menu.
2. Double click on the **Initialize Connection** button on the **Tasks** Pane.
3. Then double click on the **Link Project to Device** button. A pop-up window will appear with the information related to the design. Click the **OK** button on the pop-up window.
4. Finally, double click on the **Create Memory Interface Connection** button. Another pop-up window will appear to identify the connections. Click the **OK** button on the pop-up window.
5. Once the connection is established, scroll down the **Tasks** pane and look for the **Generate All Reports** button. Double click on it and the toolkit will generate the calibration report and summary report.
6. The reports will be available under the **Report.**

Lab Steps

The lab uses Quartus II v15.0. The lab assumes the reader is a competent user of these tools and many of their features.
Three files have been pre-design for this lab to save time:
1. A pin location assignments TCL script (*A10_pin_assignment.tcl*)
2. A custom Component Definition File of Example Design In-System Source and Probe (*ed_iss_hw.tcl*)
3. A custom RTL wrapper for Example Design In-System Source and Probe (*ed_iss.v*)
Create a new folder for the project and place the files in it.

Design Generation

1. In the Quartus II software, create a Quartus II project using the **New Project Wizard** available from the **File** menu. For this lab, use following information to setup the project accordingly:

- Working directory : <your project folder>
- Project name : ddr3
- Device name : 10AX115S2F45I1SGE2
- Leave other settings to default

2. Launch the **IP Catalog** from the **Tools** menu
3. Double click **Arria 10 External Memory Interfaces** IP from the **Memory Interfaces and Controllers** folder in the **Library** list. **IP Parameter Editor** will be launch.
4. In **New IP Variation** window, specify the **Entity name** and click **OK**. For this lab, use following information to setup the IP variation accordingly.

- Entity name : ddr3
- Leave other settings to default

5. In **Presets** window, select the preset matching or closest to the target memory device.

6. Specify the parameters on all tabs. The value should be based on the target memory device, FPGA device and board being used. For this lab, use following information to configure the remaining IP parameter that should be different than the default value or the preset.

- General tab
  - Clocks
    - Uncheck the Use recommended PLL refeerence clock frequency checkbox
    - Select 133.333MHz for the PLL reference clock frequency
- **I/O** tab (Uncheck the **Use default I/O settings** checkbox)
  - **PHY Inputs**
    - **PLL reference clock I/O standard** = LVDS (Based on Arria 10 10AX115 Pin-out file)
- **Memory Topology** tab
  - **Topology**
    - **DQ width** = 40
  - **Mode Register Settings**
    - **ODT Rtt nominal value** = RZQ/6
- **Memory Timing** tab
  - **tRRD** = 7 cycles
  - **tFAW** = 35.0 ns
- **Board Timing** tab (Based on internal board information)
  - Slew Rates
    - Use default slew rates = Checked
  - Intersymbol Interference/Crosstalk

- Board and Package Skews
    - Package deskewed with board layout (DQS group) = Unchecked
    - Maximum board skew within DQS group = 0.02 ns
    - Package deskewed with board layout (address/command bus) = Checked
    - Maximum system skew within address/command bus = 0.02 ns
    - Average delay difference between DQS and CK = 0.02 ns
    - Maximum delay difference between DIMMs/devices = 0.05 ns
    - Maximum skew between DQS groups = 0.02 ns
    - Average delay difference between address/command and CK = 0.0 ns
    - Maximum CK delay to DIMM/device = 0.6 ns
    - Maximum DQS delay to DIMM/device = 0.6 ns
- **Diagnostics** tab
    - Calibration Debug Options
        - Quartus II EMIF Debug Toolkit/On-chip Debug Port = Add EMIF Debug Interface
        - Enabled Daisy-Chaining for Quartus II EMIF Debug Toolkit/On-Chip Debug Port = Unchecked

Important Note : Review any warning messages displayed in the Messages Window and correct any errors before making further changes

Important Note : Instead of leaving it to default, ensure the parameters in **Board Timing** tab are configured correctly based on the actual target board as the value are vary from board to board. Use HyperLynx or similar simulator to obtain values of the actual target board.

Important Note : Take note on the info messages regarding which address/command pin placement scheme that need to follow based on the final IP setting. This info will be needed during pin assignment in the later stage.

Note : For **Board and Package Skews**, use Board Skew Parameter Tool available in Altera web to compute the value

Note : For detailed explanation of the parameters, refer to Parameterizing Memory Controllers with Arria 10 External Memory Interface IP chapter of the External Memory Interface Handbook.

7. Click **Example Design** button at the top-right corner of the **Parameter** window, confirm the default path for the example design, and click **OK**.
8. Once the generation completed, click **Close**.
9. Click **Finish**. The configuration is saved as *ddr3.qsys* which located inside *<your project folder>* directory.
10. Since this lab will only use the example design files, click **No** when prompted to generate your IP.
11. In **Integration with the Quartus II Software** window, click **Close**.
12. Click **Yes** when prompted to add the Quartus II IP File to the project.
13. In terminal, change directory to *<your project folder>/emif_0_example_design* folder and run following commands in sequence:

    i. $ quartus_sh -t make_qii_design.tcl

    ii. $ quartus_sh -t make_sim_design.tc

Note :Review the *readme.txt* file generated under *<your project folder>/emif_0_example_desig/qii/altera_emif_arch_nf_141/synth folder*. The file contains high-level overview, recommendation and requirements of the IP based on the selected configuration

Adding SignalTap file Into Existing Example Design

1. In the Quartus II software, launch **SignalTap II Logic Analyzer** from **Tools** menu.

    i. Under the **Signal Configuration** section, use the *pll_ref_clk* for the **Clock**

    ii. Include the following signals into your SignalTap file. Double click on the **Setup** area and search for the signals in the **Named** section on the pop-up window.

- emif_0_example_design|local_cal_fail
- emif_0_example_design|local_cal_success
- altera_emif_avl_tg_top:tg|traffic_gen_fail_0
- altera_emif_avl_tg_top:tg|traffic_gen_pass_0
- altera_emif_avl_tg_top:tg|traffic_gen_timeout_0
- loop_counter[31..0]

Implementing Additional Loop on Traffic Generator

The current traffic generator is design to run 1 loop for the example design. Changes to the RTL will be needed to enable the design to run for 10000 loop.

1. Look for the under the *altera_emif_avl_tg_driver.sv* file *altera_emif_tg_avl_150\synth* folder

2. Open this file using your choice of editor, and look for the *parameter TG_NUM_DRIVER_LOOP* section

3. Change the value for the *(TG_TEST_DURATION == "SHORT")* from the original 1 to 10000.

Design Constraint, Compilation and Analysis

1. In the Quartus II software, open the generated example design Quartus II project (ed_synth.qpf) using the **Open Project** available from the **File** menu. The Quartus II project file should be under < *your project folder >/emif_0_example_desig/qii* folder.
2. Assign the location for all top level pins. Pin locations for external memory systems are not automatically created as it depend on the individual board layout and device package being used. For this lab, do the following steps:

i. Place the *a10_pin_assignment.tcl* in < *your project folder >/emif_0_example_desig/qii*.
ii. Launch the **Tcl Scripts** from **Tools** menu.
iii. In the TCL Scripts window, select the *10a_pin_assignment.tcl* script under the Project folder in the Libraries and click Run to run the script.
iv. Click **OK** when a window appeared indicating the script has been executed and click **Close** to close the **TCL Scripts** window .
v. Verify in **Pin Planner** or **Assignment Editor** available under the **Assignments** menu to ensure the pin locations has been assigned correctly

Note: Board designer should comply with the following pin-out guideline when designing the board. To ensure the correctness, cross-check the pin location assignment with the respective document too.

- Guidelines for Arria 10 External Memory Interface IP topic under Planning Pin and FPGA Resources chapter of the External Memory Interface Handbook.
- Pin locations section in the readme.txt file generated under < your project folder >/emif_0_example_desig/qii/altera_emif_arch_nf_141/synth folder.
- Arria 10 Device Pin-Out Files on Altera web.
- Arria 10 External Memory Interface Pin Information on Altera web. Use the address/command pin placement scheme information (as in noted in Design Generation stage) to determine which column should be referred to.

3. Run full compilation by clicking the **Start Compilation** under the **Processing** menu. The compilation may take around 10 minutes to complete depending on compilation PC.
4. Once the compilation complete, ensure that there are no timing violation. There are 2 areas that should be check as below:

- In **Messages** window, ensure that "Critical Warning (332148): Timing requirements not met" message has not being printed out.
- In **Compilation Report** window, in **emif_0_example_design** table under each **TimeQuest Timing Analyzer** / **< Operating condition >** / **Report DDR** folder, ensure all number are positive. Note that this report only cover for those that are under Arria 10 External Memory Interface IP clock domain.
-

5. Review all the Critical Warnings and Warnings and determines if it is acceptable or need to be address