Intel® Xeon Phi™ Coprocessor
Architecture Overview
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Architecture Topics

- Intel® Many Integrated Core (MIC) Architecture
- Intel® Xeon Phi™ Coprocessor Overview
- Core and Vector Processing Unit
- Setting Expectations
- Performance
- Summary
Module Outline

- Intel® Many Integrated Core (MIC) Architecture
  - Intel® Xeon Phi™ Coprocessor Overview
  - Core and Vector Processing Unit
  - Setting Expectations
  - Performance
  - Summary
Intel Architecture Multicore and Manycore

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<th>Intel® Xeon® processor 64-bit</th>
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<th>Intel® Xeon® processor code name Haswell</th>
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</table>

Intel® Xeon Phi™ coprocessor extends established CPU architecture and programming concepts to highly parallel applications.

Images do not reflect actual die sizes. Actual production die may differ from images.
Intel® Multicore Architecture

- Foundation of HPC Performance
- Suited for full scope of workloads
- Industry leading performance and performance/watt for serial & parallel workloads
- Focus on fast single core/thread performance with "moderate" number of cores

Intel® Many Integrated Core Architecture

- Performance and performance/watt optimized for highly parallelized compute workloads
- Common software tools with Intel® Xeon® architecture enabling efficient application readiness and performance tuning
- Intel® Architecture extension to Manycore
- Many cores/threads with wide SIMD
Consistent Tools & Programming Models

Code → Compiler Libraries → Parallel Models → Multicore → Standards Programming Models → Vectorize, Parallelize, & Optimize → Manycore → Intel® Xeon Phi™ Coprocessor

Intel® Xeon Phi™ Coprocessor
Software & Services Group, Developer Relations Division
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Module Outline

• Intel® Many Integrated Core (MIC) Architecture

• **Intel® Xeon Phi™ Coprocessor Overview**

• Core and Vector Processing Unit

• Setting Expectations

• Performance

• Summary
Introducing Intel® Xeon Phi™ Coprocessors

*Highly-parallel Processing for Unparalleled Discovery*

**Groundbreaking differences**

- Up to 61 Intel® Architecture cores/1.1 GHz/ 244 threads
- Up to 8 GB memory with up to 352 GB/s bandwidth
- 512-bit SIMD instructions
- Linux* operating system, IP addressable

**Standard programming languages and tools**

**Leading to Groundbreaking results**

- Over 1 TeraFlop/s double precision peak performance¹
- Up to 2.2x higher memory bandwidth than on an Intel® Xeon® processor E5 family-based server²
- Up to 4x more performance per watt than with an Intel Xeon processor E5 family-based server³
Intel® Xeon Phi™ Architecture Overview

Cores: 61 cores, at 1.1 GHz in-order, support 4 threads
512 bit Vector Processing Unit
32 native registers

High-speed bi-directional ring interconnect
Fully coherent L2 Cache

Distributed tag directory to uniquely map physical addresses

Parity on L1 Cache, ECC on memory
CRC on memory IO, CAP on memory IO

Reliability Features

8 memory controllers
16-channel GDDR5 MC
PCIe GEN2

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Core Architecture Overview

- 60+ in-order, low-power Intel® Architecture cores in a ring interconnect
- Two pipelines
  - Scalar Unit based on Pentium® processors
  - Dual issue with scalar instructions
  - Pipelined one-per-clock scalar throughput
- SIMD Vector Processing Engine
- 4 hardware threads per core
  - 4 clock latency, hidden by round-robin scheduling of threads
  - Cannot issue back-to-back inst in same thread
- Coherent 512 KB L2 Cache per core
Core Architecture Overview

- 2 issue (1 scalar/1 vector)
- 2 cycle decoder: no back-to-back cycle issue from the same context (thread)
- Most vec instructions have 4 clock latency
- At least two HW contexts (thread/proc) to fully utilize the core
Core Architecture Overview

- Performance Monitoring Unit
  - 4 event select register
  - 4 performance counters
  - Shared among the 4 HW threads
  - Programmable via model specific registers (MSR) using RDMSR/WRMSR
Knights Corner Architecture Overview – Cache

352 GB/s BW (theoretical)
Knights Corner Architecture Overview

– Cache

• L1 cache
  – 32K I-cache per core
  – 32K D-cache per core
  – 8 way associative
  – 64B cache line
  – 3 cycle access
  – Up to 8 outstanding requests
  – Fully coherent (MESI)

• L2 cache
  – 512K Unified per core
  – 8 way assoc
  – Inclusive
  – 31M total across 62 cores
  – 11 cycle best access
  – Up to 32 outstanding requests
  – Streaming HW prefetcher
  – Fully coherent
Knights Corner Architecture Overview

- **Cache**

- **Alignment**
  - Based upon number of elements, element size, and vector load and store instruction
  - 64B alignment for 4B (float) data elements for a 16 to 16 vector load

- **Memory**
  - 8GB GDDR5
  - 8 Memory controllers, 16 GDDR5 channels, up to 5.5 GT/s
  - 300 ns access
  - Aggregate 352 GB/s peak memory bandwidth
  - ECC

- **PCI Express***
  - Gen2 (Client) x16 per direction
Module Outline

• Intel® Many Integrated Core (MIC) Architecture
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• Performance
• Summary
Knights Corner Architecture Overview
Vector Processing Unit and ISA

SSE
- 128 bit
- 2 x DP
- 4 x SP

AVX
- 256 bit
- 4 x DP
- 8 x SP

MIC
- 512 bit
- 8 x DP
- 16 x SP

Not part of Intel® Xeon Phi™ coprocessor
Vector Processing Unit Extends the Scalar IA Core

Instruction Cache Miss

Thread 0 IP → L1 TLB and L1 instruction cache 32KB → Decoder → L1 TLB and L1 Data Cache 32 KB

Pipe 0 (u-pipe) → VPU RF

Thread 1 IP → Pipe 1 (v-pipe) → uCode → L1 TLB and L1 Data Cache 32 KB

Pipe 2 IP

Thread 3 IP

PPF PF D0 D1 D2 E WB

TLB Miss Handler → L2 TLB

HWP L2 CRI

512KB L2 Cache

On-Die Interconnect

16B/cycle (2 IPC)

4 threads in order

Thread 0 IP

Thread 1 IP

Thread 2 IP

Thread 3 IP

VPU RF

X87 RF

Scalar RF

VPU 512b SIMD

X87

ALU 0

ALU 1

L1 TLB and L1 Data Cache 32 KB

TLB miss

Data Cache Miss
Vector Processing Unit and Intel® Initial Many Core Instructions (Intel® IMCI)

- Vector Processing Unit Execute Intel IMCI
- 512-bit Vector Execution Engine
  - 16 lanes of 32-bit single precision and integer operations
  - 8 lanes of 64-bit double precision and integer operations
  - 32 512-bit general purpose vector registers in 4 thread
  - 8 16-bit mask registers in 4 thread for predicated execution
- Read/Write
  - One vector length (512-bits) per cycle from/to Vector Registers
  - One operand can be from memory
- IEEE 754 Standard Compliance
  - 4 rounding models, even, 0, +∞, -∞
  - Hardware support for SP/DP denormal handling
  - Sets status register VXCSR flags but not hardware traps
Vector Instruction Performance

• VPU contains 16 SP ALUs, 8 DP ALUs

• Most VPU instructions have a latency of 4 cycles and TPT 1 cycle
  – Load/Store/Scatter have 7-cycle latency
  – Convert/Shuffle have 6-cycle latency

• VPU instruction are issued in u-pipe

• Certain instructions can go to v-pipe also
  – Vector Mask, Vector Store, Vector Packstore, Vector Prefetch, Scalar
Module Outline

- Intel® Many Integrated Core (MIC) Architecture
- Intel® Xeon Phi™ Coprocessor Overview
- Core and Vector Processing Unit
- Software Ecosystem
- Performance
- Summary
Programming Considerations - Setting Expectations (1)

• Getting full performance from the Intel® MIC architecture requires both a high degree of parallelism and vectorization
  – Not all code can be written this way
  – Not all programs make sense on this architecture

• The Intel® Xeon® processor is not an Intel® Xeon® processor
  – It specializes in running highly parallel and vectorized code
  – New vector instruction set and 512-bit wide registers
  – Not optimized for processing serial code
Programming Considerations - Setting Expectations (2)

- Coprocessor comes with 8 GB of memory
  - Only ~7 GB is available to your program
    o The other ~1GB is used for data transfer and is accessible to your coprocessor code as buffers.

- Very short (low-latency) tasks not optimal for offload to the coprocessor
  - Costs that you need to amortize to make it worthwhile:
    o Code and data transfer
    o Process/thread creation
  - Fastest data transfers currently require careful data alignment

- This architecture is not optimized for serial performance
Intel® MIC Programming Considerations – This is not a GPU

- Very different memory architectures
  - The Intel MIC Architecture is not optimized for concurrent out-of-cache random memory accesses by large numbers of threads (GPUs are)
  - The Intel MIC Architecture has a “traditional” coherent-cache architecture
  - GPUs have a memory architecture specialized for localized “shared memory” processing

- “Threads” and “cores” mean something very different - GPU versions of these are limited and lighter-weight

- Each architecture (host CPU, Intel MIC Architecture, or GPU) is really good at some things, and not others
  - Because the Intel MIC Architecture is similar to the Intel® Xeon® processor, probably your best choice for further accelerating highly parallel and vectorized code developed on Intel Xeon processor
Module Outline

- Intel® Many Integrated Core (MIC) Architecture
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- Setting Expectations

- **Performance**
- Summary
Theoretical Maximum
(Intel® Xeon® processor E5-2670 vs. Intel® Xeon Phi™ coprocessor 5110P & SE10P/X)

Single Precision (GF/s)
Up to 3.2x
Higher is Better

Double Precision (GF/s)
Up to 3.2x
Higher is Better

Memory Bandwidth (GB/s)
Up to 3.45x
Higher is Better

Synthetic Benchmark Summary

**SGEMM (GF/s)**
- E5-2670 Baseline: 640, 85% Efficient
- 5110P: 1,729, 86% Efficient
- SE10P: 1,860, 86% Efficient
- Up to 2.9X

**DGE MM (GF/s)**
- E5-2670 Baseline: 309, 82% Efficient
- 5110P: 833, 82% Efficient
- SE10P: 883, 82% Efficient
- Up to 2.8X

**SMP Linpack (GF/s)**
- E5-2670 Baseline: 303, 71% Efficient
- 5110P: 722, 75% Efficient
- SE10P: 803, 75% Efficient
- Up to 2.6X

**STREAM Triad (GB/s)**
- E5-2670 Baseline: 80, ECC On
- 5110P: 159, ECC On
- SE10P: 174, ECC On
- Up to 2.2X

Coprocessor results: Benchmark runs 100% on coprocessor, no help from Intel® Xeon® processor host (aka native). For more information go to http://www.intel.com/performance
Intel® Xeon Phi™ Coprocessor vs. Intel® Xeon® Processor

Financial Services Workloads

Higher is Better

Relative Performance (Normalized to 1.0 Baseline of a 2 socket Intel® Xeon® processor)

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<th>Workload</th>
<th>2S Intel® Xeon® Processor</th>
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1. 2X Intel® Xeon® Processor E5-2670 (2.6GHz, 8C, 115W)
2. Intel® Xeon Phi™ coprocessor SE10 (ECC on) with pre-production SW stack

Higher SP results are due to certain Single Precision transcendental functions in the Intel® Xeon Phi™ coprocessor that are not present in the Intel® Xeon® processor.
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Architecture Summary

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Intel® Xeon Phi™ Coprocessor Workshop
Pawsey Centre & CSIRO, Aug 2013

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