Intended Audience: Software Developers

• Interested in performance optimizing your application
  > Don’t need to be a performance expert
  > But should be an expert in the application!

• Working on a platform with a 4th generation Intel® Core™ processor

• Using Intel® VTune™ Amplifier XE performance analyzer
  > The performance information here applies to other tools (PTU, etc) but is focused on VTune Amplifier XE
How to Use this Presentation

- Read through the slides once, then again while collecting data
- Remember performance analysis is a process that may take several iterations
- Software Optimization should begin after you have:
  - Utilized any compiler optimization options (/O2, /QxAVX, etc)
  - Chosen an appropriate workload
  - Measured baseline performance
Using Intel® VTune™ Amplifier XE to Tune Software on the 4th generation Intel® Core™ processor family

Software and Services Group

Ver. 1.0
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Notice revision #20110804
Agenda

– The 4th generation Intel® Core™ processor
– The new Intel® VTune™ Amplifier XE
– The Software Optimization Cycle
  > Hotspots
  > Methods for Determining Efficiency
– Tuning Suggestions
  > Tuning for Front-End Bound
  > Tuning for Back-End Bound
  > Tuning for Bad Speculation
  > Tuning for Retiring
For more information, see http://www.intel.com/content/www/us/en/processors/core/core-processor-family.html
Some Performance Features of the 4th generation Intel® Core™ Processor Family

- Manufactured on Intel® 22nm process technology – delivering a performance and energy boost
- Intel® Turbo Boost 2.0 Technology
- Intel® Hyper-Threading Technology
- Intel® Advanced Vector Extensions (AVX) and Intel® Advanced Vector Extensions 2 (AVX2) Instructions
- Intel® Smart Cache
- Intel® Quick Sync Video
- Intel® Clear Video HD
- Intel® InTru™ 3D

Uses Haswell microarchitecture
The New Intel® VTune™ Amplifier XE

VTune Amplifier XE 2013 features:
- Multiple Collection Types
  > Hotspots (statistical call tree)
  > Thread Concurrency
  > Locks and Waits Analysis
  > Event-based Sampling
- Timeline View Integrated into all Analysis Types
- Source/Assembly Viewing
- Compatible with C/C++, Fortran, Java, Assembly, .NET
- Visual Studio Integration, Command-line, or Standalone interface for Windows* or Linux*
The logic for identifying issues on the Haswell microarchitecture is embedded into the interface. All the formulas and metrics used are the same as the ones given in this guide. You no longer have to apply formulas and rules to the data yourself to figure out what it means – using this guide and the interface tuning features, you can easily pinpoint problems and possible solutions.

The formulas and metrics are only applied to the General Exploration profile, and the General Exploration viewpoint (which is automatic). For the other profiles, it will just show the raw data.
The enhanced view is present when running the General Exploration profile with the General Exploration viewpoint selected (the default).

All collected data is presented in hierarchical format (see next slide), with helpful metrics already calculated (see issue slides).
### Enhanced General Exploration View for Haswell microarchitecture

**Diagram Description:**
- A hierarchical data display corresponds to how available execution slots in each core's pipeline are utilized.
- Expand a column to see a breakdown of issues pertaining to its category of pipeline utilization: Retiring, Bad Speculation, Back-end Bound, or Front-end Bound Pipeline Slots.

**Table Data:**
- | Function | Hardware Execs | Hardware Evictions | Filled Pipeline Slots Retiring | Filled Pipeline Slots Bad Speculation | Filled Pipeline Slots Back-end Bound | Filled Pipeline Slots Front-end Bound |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>end_intercept</td>
<td>7,062,000,000</td>
<td>10,040,000,000</td>
<td>0.750</td>
<td>0.147</td>
<td>0.425</td>
<td>0.129</td>
</tr>
<tr>
<td>sphere_intercept</td>
<td>7,676,000,000</td>
<td>10,258,000,000</td>
<td>0.740</td>
<td>0.347</td>
<td>0.132</td>
<td>0.524</td>
</tr>
<tr>
<td>rigid_bounds_intercept</td>
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<td>426,000,000</td>
<td>0.345</td>
<td>0.174</td>
<td>0.157</td>
<td>0.462</td>
</tr>
<tr>
<td>gdpCreateGdpFp</td>
<td>690,000,000</td>
<td>247,000,000</td>
<td>1.360</td>
<td>0.367</td>
<td>0.060</td>
<td>0.711</td>
</tr>
<tr>
<td>I/O Scheduler</td>
<td>280,000,000</td>
<td>72,000,000</td>
<td>2.889</td>
<td>0.268</td>
<td>0.000</td>
<td>0.071</td>
</tr>
<tr>
<td>msdos</td>
<td>238,000,000</td>
<td>324,000,000</td>
<td>1.963</td>
<td>0.221</td>
<td>0.200</td>
<td>0.527</td>
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<td>[ntoskrnl.dll]</td>
<td>238,000,000</td>
<td>514,000,000</td>
<td>0.459</td>
<td>0.456</td>
<td>0.117</td>
<td>0.000</td>
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<td>pshmem</td>
<td>196,000,000</td>
<td>239,000,000</td>
<td>0.446</td>
<td>0.394</td>
<td>0.113</td>
<td>0.699</td>
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<td>142,000,000</td>
<td>1.239</td>
<td>0.227</td>
<td>0.000</td>
<td>0.815</td>
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<td>270,000,000</td>
<td>0.511</td>
<td>0.540</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>intersect_objects</td>
<td>86,000,000</td>
<td>58,000,000</td>
<td>1.403</td>
<td>0.116</td>
<td>0.016</td>
<td>0.223</td>
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<tr>
<td>#more</td>
<td>80,000,000</td>
<td>64,000,000</td>
<td>1.250</td>
<td>0.250</td>
<td>0.000</td>
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<tr>
<td>#more</td>
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<td>10,040,000,000</td>
<td>0.150</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

*Note: The data reflects performance metrics for various functions and execution slots.*
Note that issue highlighting occurs under 2 conditions:

1. The value for the metric is over VTune’s pre-determined threshold

2. The associated function uses 5% or greater of the CPU clockticks sampled
Both Intel® Hyper-Threading Technology and Intel® Turbo Boost 2.0 Technology can be enabled or disabled through BIOS on most platforms.

Contact the system vendor or manufacturer for the specifics of any platform before attempting this. Incorrectly modifying bios settings from those supplied by the manufacturer can result in rendering the system completely unusable and may void the warranty.

Don’t forget to re-enable these features once you are through with the software optimization process!
The “Software on Hardware” Tuning Process

For each Hotspot

– Determine efficiency
  > If inefficient:
    • Determine primary bottleneck
    • Identify architectural reason for inefficiency
    • Optimize the issue

Repeat

Note: While VTune Amplifier XE’s Concurrency, Timeline and Locks and Waits features can also be helpful in threading an application, this slideset is not aimed at the process of introducing threads.

The process described here could be used either before or after threading.

However, we *do* recommend that you follow a top-down process when optimizing: beginning with system tuning (if appropriate), then algorithmic tuning, then microarchitectural tuning. The name of Software on Hardware tuning just means we are tuning software for specific hardware.

Remember for all upcoming slides – that you should only focus on hotspots! Only try to determine efficiency, identify causes, and optimize in hotspots!
The “Software on Hardware” Tuning Process

For each Hotspot
  – Determine efficiency
    > If inefficient:
      • Determine primary bottleneck
      • Identify architectural reason for inefficiency
      • Optimize the issue

Repeat
For the 4\textsuperscript{th} Generation Intel Core processor family, the CPU\_CLK\_UNHALTED.THREAD counter measures unhalted clockticks on a per thread basis. So for each tick of the CPU's clock, the counter will count 2 ticks if Hyper-Threading is enabled, 1 tick if Hyper-Threading is disabled. There is no per-core clocktick counter.

There is also a CPU\_CLK\_UNHALTED.REF counter, which counts unhalted clockticks per thread, at the reference frequency for the CPU. In other words, the CPU\_CLK\_UNHALTED.REF counter should not increase or decrease as a result of frequency changes due to Turbo Mode 2.0 or Speedstep Technology.
The "Software on Hardware" Tuning Process

For each Hotspot

- Determine efficiency
  - If inefficient:
    - Determine primary bottleneck
    - Identify architectural reason for inefficiency
    - Optimize the issue

Repeat
Determine Efficiency

- Determine efficiency of the hotspot using one of three methods:
  - % Pipeline Slots Retiring
  - Changes in CPI
  - Code Examination

- Note: Some of these methods are more appropriate for certain codes than others... see notes on the following slides

% Pipeline Slots Retired and Changes in CPI methods rely on VTune Amplifier XE's event-based sampling. The Code Examination method relies on using VTune Amplifier XE's capability as a source/disassembly viewer.
**Efficiency Method 1: % Retiring Pipeline Slots**

- **Why:** Helps you understand how efficiently your app is using the processors
- **How:** General Exploration profile, Metric: Retiring
- **What Now:**
  - For a given hotspot:
    - If 75% or more of pipeline slots are retiring (.75 or higher), Go to efficiency method 3, code study 1 – to see if vectorization can boost performance further
  - Otherwise, see next slide

**Formula:**

\[
\frac{UOPS\_RETIRED\_RETIRE\_SLOTS}{4 \times CPU\_CLK\_UNHALTED\_THREAD}\]

**Thresholds:** Investigate if -

- % Retiring < .75

This metric is based on the fact that when operating at peak performance, the pipeline on a Haswell CPU should be able to retire 4 micro-operations per clock cycle (or “clocktick”). The formula looks at “slots” in the pipeline for each core, and sees if the slots are filled, and if so, whether they contained a micro-op that retired. More details on this methodology are available in the coming slides or in this paper: [http://software.intel.com/en-us/articles/how-to-tune-applications-using-a-top-down-characterization-of-microarchitectural-issues](http://software.intel.com/en-us/articles/how-to-tune-applications-using-a-top-down-characterization-of-microarchitectural-issues)
The thresholds are general guidelines. Depending on the domain, some applications can run with less slots retiring than the thresholds above and still be efficient. It is important to remember that the pipeline slot methodology is only looking at how a given code utilizes the pipeline on a core. There still may be algorithmic optimizations, like parallelism and vectorization, that would boost the application’s performance.
Formula:

\[
\frac{\text{CPU_CLK_UNHALTED.THREAD}}{\text{INST RETIRED.ANY}}
\]

Threshold:

In the interface, CPI will be highlighted if > 1. This is a very general rule based on the fact that some well-tuned apps achieve CPIs of 1 or below. However, many apps will naturally have a CPI of over 1 – it is very dependent on workload and platform. It is best used as a comparison factor – know your app’s CPI and see if over time it is moving upward (that is bad) or reducing (good!).

Note that CPI is a ratio! Cycles per instruction. So if the code size changes for a binary, CPI will change. In general, if CPI reduces as a result of optimizations, that is good, and if it increases, that is bad. However, there are exceptions! Some code can have a very low CPI but still be inefficient because more instructions are executed than are needed. This problem is discussed using the Code Examination method for determining efficiency.

Another Note: CPI will be doubled if using Intel® Hyper-threading. With Intel® Hyper-Threading enabled, there are actually 2 different definitions of CPI. We call them "Per Thread CPI" and "Per Core CPI". The Per Thread CPI will be twice the Per Core CPI. Only convert between per Thread and per Core CPI when viewing aggregate CPIs (summed for all logical threads).

Note: Optimized code (i.e.: SSE instructions) may actually lower the CPI, and increase stall % – but it will increase the performance. CPI is just a general efficiency metric – the real measure of efficiency is work taking less time.
Efficiency Method 3: Code Examination

- **Why:** Methods 1 and 2 measure how long it takes instructions to execute. The other type of inefficiency is executing too many instructions.
- **How:** Use VTune Amplifier XE’s capability as a source and disassembly viewer
- **What Now:**
  - Failure to utilize modern instructions results in larger code size
  - See next 3 slides for potential issues

This method involves looking at the disassembly to make sure the most efficient instruction streams are generated. This can be complex and can require an expert knowledge of the Intel instruction set and compiler technology. What we have done is describe how to find 3 easy-to-detect code patterns and suggest how they may be implemented more efficiently using new features of the Intel Haswell CPU.

For more on vectorization in general: http://software.intel.com/en-us/articles/vectorization-toolkit

SSE instructions will look like: addps xmm4, xmm5.

+ addss is a s(calar) Intel® SSE instruction – packed SSE instructions such as addps are a better choice
Note that FMA instructions perform a multiply, add, and round. A multiply followed by an add would have 2 rounds (one after the multiply and one after the add). Since the FMA eliminates the intermediate rounding operation, results may be different when using FMAs as opposed to multiplies followed by adds. For more information, see the Intel® 64 and IA-32 Architectures Software Developer’s Manual at [http://download.intel.com/products/processor/manual/325462.pdf](http://download.intel.com/products/processor/manual/325462.pdf), section 13.5.

- **Why:** Intel AES-NI can accelerate the execution of AES algorithms by implementing some of the functionality in hardware

- **How:** If the application’s implements AES algorithms, check to see if Intel AES-NI instructions are being used. Blocks of aes instructions with xmm registers as operands may be using parallel modes:

  - `aesenc %xmm5, %xmm7`
  - `aesenc %xmm5, %xmm8`
  - `aesenc %xmm5, %xmm9`
  - `aesenc %xmm5, %xmm10`

- **What Now:**
  - If AES-NI are being used in parallel modes (such as ECB, CTR, and CBC-Decrypt), increase performance by redefining the number of blocks to be processed in parallel (8 on Haswell).
The “Software on Hardware” Tuning Process

For each Hotspot

- Determine efficiency
  > If inefficient:
    - Determine primary bottleneck
    - Identify architectural reason for inefficiency
    - Optimize the issue

Repeat
For a hotspot that is inefficient, determining the primary bottleneck is the first step. Optimizing code to fix issues outside the primary bottleneck category may not boost performance – the biggest boost will come from resolving the biggest bottleneck. Generally, if Retiring is the primary bottleneck, that is good. See next slides.
A Pipeline slot is an abstract concept – it represents the hardware resources needed to process one micro-operation.

On Haswell, there are 4 pipeline slots available on each core, each cycle.

Performance is classified according to what happened for each slot available to the application or hotspot:

1. **Was a Micro-op Issued?**
   - Yes: Did Micro-op Retire?
     - Yes: Retiring
     - No: Bad Speculation
   - No: Allocation Stall?
     - Yes: Back-End Bound
     - No: Front-End Bound

Note that the way this methodology allows us to classify what percentage of all pipeline slots end up in each category, for each cycle and for each core. It is possible that for a given dataset, there may be a significant percentage of pipeline slots in multiple categories that merit investigation. Start with the category with the highest percentage of pipeline slots. Ideally a large percentage of slots will fall into the “Retired” category, but even then, it may be possible to make your code more efficient.

For a complete description of this methodology, see the Intel® 64 and IA-32 Architectures Optimization Reference Manual, Appendix B.3.
The distribution of pipeline slots in these four categories is very useful for developers. Although metrics based on events have been possible for many years, before this characterization there was no approach for identifying which possible performance issues were the most impactful. When performance metrics are placed into this framework, a developer can see which issues need to be tackled first. Within VTune Amplifier XE, if an issue is highlighted, it doesn’t need to be investigated unless it is from the primary bottleneck category. Fixing issues that are not within the primary bottleneck category may not improve performance.
The “Software on Hardware” Tuning Process

For each Hotspot

- Determine efficiency
  > If inefficient:
    • Determine primary bottleneck
    • Identify architectural reason for inefficiency
    • Optimize the issue

Repeat
Identifying Architectural Reasons for Inefficiency: The Issue Slides

- Issues are listed by category, and each category is explained.
- For each potential issue, there are several important pieces of information:
  - Why? – Why you should be concerned about this potential problem.
  - How? – Which profile and metric to use in the Amplifier XE interface. If the data is highlighted, then it should be investigated.
  - What Now? – Helps you **Optimize the Issue**. Gives suggestions for follow-up investigations or optimizations to try.
  - Event Names and Metric Formulas are given in the Notes. These are not included on the slide because they are already embedded in the Amplifier XE logic. You only need to use the pre-configured profiles and metrics pointed out in order to know if you may have a problem.
Tuning for the Front-End Bound Category

The Front-End of the pipeline
- Fetches instructions
- Decodes instructions into micro-operations
- Delivers up to 4 micro-operations per cycle to the Back-End
Front-End issues are caused by delays in fetching code (due to caching or ITLB issues) or in decoding instructions (due to specific instruction types or queueing issues). Front-End issues are generally resolved by compiler techniques like code layout (co-locating hot code), reducing code footprint, and Profile-Guided Optimization (PGO).
Front-End Hierarchical Breakdown in Amplifier XE

Expand Front-End Bound to see the percentage of the Front-End Bound cycles classified as "Front-End Latency", where no micro-ops were being delivered, vs "Front-End Bandwidth", where <4 micro-ops were being delivered.

If Front-End Bound is the primary bottleneck, concentrate on Front-End Latency. Resolve highlighted issues under this category.
Formulas:

% of cycles spent on ITLB Misses (ITLB Overhead):
\[
\frac{\text{ITLB\_MISSES\_WALK\_DURATION}}{\text{CPU\_CLK\_UNHALTED\_THREAD}}
\]

% of cycles spent on iCache Misses (Icache Overhead):
\[
\frac{(36\times\text{ICACHE\_MISSES})}{\text{CPU\_CLK\_UNHALTED\_THREAD}}
\]

% of cycles due to LCP stalls:
\[
\frac{\text{ILD\_STALL\_LCP}}{\text{CPU\_CLK\_UNHALTED}}
\]

Thresholds:
Thresholds: Investigate if –
% of cycles spent on ITLB Misses (ITLB Overhead) ≥ .5 (5%)
% of cycles spent on ICache Misses (ICache Overhead) ≥ .5 (5%)
% of cycles due to LCP stalls ≥ .5 (5%)
Tuning for the Back-End Bound Category

The Back-End of the pipeline
- Accepts micro-operations from the Front-End
- Re-orders them as necessary to schedule their execution in execution units
- Retrieves needed operands from memory
- Executes the operations
- Commits results to memory
The back-end is the most common category for hotspots, and is most likely to be the primary bottleneck.
Several issues can result in Memory Bound time in the Back-End. If greater than 50% of Back-End time is spent Memory Bound, investigate any highlighted issues. If greater than 50% of time is spent Core Bound, see slide xx.

Expand Back-End Bound to see the percentage of all cycles in the Back-End classified as “Memory Bound”, where the back-end could not accept new micro-ops due to too many outstanding memory operations, vs “Core Bound”, where the issue is saturation execution ports.
Formulas:

% of cycles spent on memory access (LLC misses):
\[
\frac{(\text{MEM\_LOAD\_UOPS\_L3\_MISS\_RETIRED.\text{LOCAL\_DRAM} \times 180})}{\text{CPU\_CLK\_UNHALTED.\text{THREAD}}}
\]

% of cycles spent on last level cache access (2nd level misses that hit in LLC):
\[
\frac{((\text{MEM\_LOAD\_RETIRED.L3\_HIT\_PS \times 36}) + (\text{MEM\_LOAD\_UOPS\_L3\_HIT\_RETIRED.XSNP\_HIT\_PS \times 72}) + (\text{MEM\_LOAD\_UOPS\_L3\_HIT\_RETIRED.XSNP\_HITM\_PS \times 84}))}{\text{CPU\_CLK\_UNHALTED.\text{THREAD}}}
\]

Thresholds: Investigate if –

% cycles for LLC miss ≥ .2,
% cycles for LLC Hit ≥ .2

LLC stands for “last level cache”, and is the L3 cache on the 4th Generation Intel Core processor family. All accesses that miss the L3 cache are counted here as an LLC miss, regardless of whether the data was found in local memory, remote memory, or a remote cache. For the LLC hit formula, it includes standard hits to the L3 as well as hits that required snoops of local L2 caches.
Contested Accesses

**Why:** Sharing modified data among cores (at L2 level) can raise the latency of data access

**How:** Memory Bound sub-category, Metric: *Contested Accesses*

**What Now:**
- If this metric is highlighted for your hotspot, locate the source code line(s) that is generating HITMs by viewing the source. Look for the MEM_LOAD_UOPS_L3_HIT RETIRED.XSNP_HITM_PS event which will tag to the next instruction after the one that generated the HITM.
- Then use knowledge of the code to determine if real or false sharing is taking place. Make appropriate fixes:
  - For real sharing, reduce sharing requirements
  - For false sharing, pad variables to cacheline boundaries

Formula:

% of cycles spent accessing data modified by another core:

\[
\frac{(\text{MEM\_LOAD\_UOPS\_L3\_HIT\_RETIRED.XSNP\_HITM\_PS} \times 84)}{\text{CPU\_CLK\_UNHALTED.THREAD}}
\]

Thresholds: Investigate if –

% cycles accessing modified data > .05

This metric is also called write sharing. It occurs when one core needs data that is found in a modified state in another core’s cache. This causes the line to be invalidated in the holding core’s cache and moved to the requesting core’s cache. If it is written again and another core requests it, the process starts again. The cacheline ping pong-ing between caches causes longer access time than if it could be simply shared amongst cores (as with read-sharing).

Write sharing can be caused by true sharing, as with a lock or hot shared data structure, or by false sharing, meaning that the cores are modifying 2 separate pieces of data stored on the same cacheline. This metric measures write sharing at the L2 level only – that is, within one socket. If write sharing is observed at this level it is possible it is occurring across sockets as well.

Note that in the case of real write sharing that is caused by a lock, Amplifier XE’s Locks and Waits analysis should also indicate a problem. This hardware-level analysis will detect other cases as well though (such as false sharing or write sharing a hot data structure).
Data Sharing

**Why:** Sharing clean data (read sharing) among cores (at L2 level) has a penalty at least the first time due to coherency

**How:** Memory Bound sub-category, Metrics: Data Sharing

**What Now:**
- If this metric is highlighted for your hotspot, locate the source code line(s) that is generating HITMs by viewing the source. Look for the MEM_LOAD_UOPS_L3_HIT_RETIRED.XSNP_HIT_PS event which will tag to the next instruction after the one that generated the HITM.
- Then use knowledge of the code to determine if real or false sharing is taking place. Make appropriate fixes:
  - For real sharing, reduce sharing requirements
  - For false sharing, pad variables to cacheline boundaries

Formula:
\[
\frac{(\text{MEM\_LOAD\_UOPS\_L3\_HIT\_RETIRED.XSNP\_HIT\_PS} \times 72)}{\text{CPU\_CLK\_UNHALTED.THREAD}}
\]

Thresholds: Investigate if –
- % cycles accessing clean shared data > .05

This metric measures read sharing, or sharing of “clean” data, across L2 caches within 1 CPU socket. The L3 cache has a set of “core valid” bits that indicate whether each cacheline could be found in any L2 caches on the same socket, and if so, which ones. The first time a line is brought into the L3 cache, it will have core valid bits set to 1 for whichever L2 cache it went into. If that line is then read by a different core, then it will be fetched from L3, where the core valid bits will indicate it is present in one other core. The other L2 will have to be snooped, resulting in a longer latency access for that line. This metric measures the impact of that additional access time, when the cacheline in question is only being read-shared. In the case of read-sharing, the line can co-exist in multiple L2 caches in shared state, and for future accesses more than one core valid bit will be set. Then when other cores request the line, no L2 caches will need to be snooped, because the presence of 2 or more core valid bits tells the LLC that the line is shared (for reading) and ok to serve. Thus the impact of this only happens the first time a cacheline is requested for reading by a second L2 after it has already been placed in the L3 cache. The impact of sharing modified data across L2s is different and is measured with the “Contested Accesses” metric.
Other Data Access Issues: Blocked Loads Due to No Store Forwarding

- **Why:** If it is not possible to forward the result of a store through the pipeline, dependent loads may be blocked
- **How:** Memory Bound sub-category, Metric: *Loads Blocked by Store Forwarding*
- **What Now:**
  - If the metric is highlighted for your hotspot, investigate:
  - View source and look at the LD_BLOCKS_STORE_FORWARD event. Usually this event tags to next instruction after the attempted load that was blocked. Locate the load, then try to find the store that cannot forward, which is usually within the prior 10-15 instructions. The most common case is that the store is to a smaller memory space than the load. Fix the store by storing to the same size or larger space as the ensuing load.

**Formula:**

Blocked Store Forwarding Cost = \( \frac{(LD\_BLOCKS\_STORE\_FORWARD \times 13)}{CPU\_CLK\_UNHALTED\_THREAD} \)

**Threshold:** Investigate if –

Cost ≥ .05

Store forwarding occurs when there are two memory instructions in the pipeline, a store followed by a load from the same address. Instead of waiting for the data to be stored to the cache, it is “forwarded” back along the pipeline to the load instruction, saving a load from the cache. Store forwarding is the desired behavior, however, in certain cases, the store may not be able to be forwarded, so the load instruction becomes blocked waiting for the store to write to the cache and then to load it.
A cacheline split is any load or store that traverses a 64-byte boundary.

Formulas:
Split Load Cost = (MEM_UOP RETIRED.SPLIT LOADS PS * 5) / CPU_CLK_UNHALTED.THREAD

Split Store Ratio = MEM_UOP RETIRED.SPLIT STORES PS / MEM_UOP RETIRED.ANY STORES PS

Thresholds: Investigate if -
Split load cost ≥ .1 or
Split store ratio is > 0.01

Beginning with the Intel® Core™ architecture, the penalty for cacheline splits has been reduced to only 5 cycles. However, if there are repeated splits occurring, the penalty can grow, and even just a 5-cycle increase in latency can make a difference in application performance.
Other Data Access Issues: 4K Aliasing

- **Why:** Aliasing conflicts result in having to re-issue loads.
- **How:** Memory Bound sub-category, Metric: 4K Aliasing
- **What Now:**
  - If this metric is highlighted for your hotspot, investigate at the sourcecode level.
  - Fix these issues by changing the alignment of the load. Try aligning data to 32 bytes, changing offsets between input and output buffers (if possible), or using 16-Byte memory accesses on memory that is not 32-Byte aligned.

**Formula:**

\[
\text{Aliasing Conflicts Cost} = \frac{(\text{LD\_BLOCKS\_PARTIAL.AADDRESS\_ALIAS} \times 5)}{\text{CPU\_CLK\_UNHALTED.THREAD}}
\]

**Threshold:** Investigate if

Aliasing conflicts cost ≥ .1

This occurs when a load is issued after a store and their memory addresses are offset by (4K). When this is processed in the pipeline, the issue of the load will match the previous store (the full address is not used at this point), so pipeline will try to forward the results of the store and avoid doing the load (this is store forwarding). Later on when the address of the load is fully resolved, it will not match the store, and so the load will have to be re-issued from a later point in the pipe. This has a 5-cycle penalty in the normal case, but could be worse in certain situations, like with un-aligned loads that span 2 cache lines.
Other Data Access Issues: DTLB Misses

- **Why:** First-level DTLB Load misses (Hits in the STLB) incur a latency penalty. Second-level misses require a page walk that can affect your application’s performance.

- **How:** Memory Bound sub-category, Metric: *DTLB Overhead, DTLB Store Overhead*

- **What Now:**
  - If this metric is highlighted for your hotspot, investigate at the sourcecode level.
  - To fix these issues, target data locality to TLB size, use the Extended Page Tables (EPT) on virtualized systems, try large pages (database/server apps only), increase data locality by using better memory allocation or Profile-Guided Optimization.

Formula:

\[
\text{DTLB Overhead} = \frac{((\text{DTLB LOAD MISSES.STLB_HIT} \times 7) + \text{DTLB LOAD MISSES.WALK DURATION})}{\text{CPU_CLK_UNHALTED.THREAD}}
\]

Threshold: Investigate if-

DTLB Overhead ≥ .1

On target data locality to TLB size: this is accomplished via data blocking and trying to minimize random access patterns.

Note: this is more likely to occur with server applications or applications with a large random dataset.
Max theoretical bandwidth, per socket, for 4th Generation Intel Core Processor Family, with DDR 1600 and 2 memory channels: 25.6 GB/s
View both total and read memory bandwidth per socket, over time.
Tuning for the Bad Speculation Category

Speculation is when:
- A micro-operation is allowed to execute, before it is known whether that operation will retire
- Allows for greater Instruction-Level Parallelism in an out-of-order pipeline
Micro-operations that are removed from the Back-End most likely happen because the Front-End mis-predicted a branch. This is discovered in the Back-End when the branch operation is executed. At this point, if the target of the branch was incorrectly predicted, the micro-operation and all subsequent incorrectly predicted operations are removed and the Front-End is re-directed to begin fetching instructions from the correct target.
Branch Mispredicts

Why: Mispredicted branches cause pipeline inefficiencies due to wasted work or instruction starvation (while waiting for new instructions to be fetched)

How: General Exploration Profile, Metric: Branch Mispredict

What Now:
- If this metric is highlighted for your hotspot try to reduce misprediction impact:
- Use compiler options or profile-guided optimization (PGO) to improve code generation
- Apply hand-tuning by doing things like hoisting the most popular targets in branch statements.

Formula:
Mispredicted branch cost: \( \frac{(20 \times BR\_MISP\_RETIRED.ALL\_BRANCHES\_PS)}{CPU\_CLK\_UNHALTED.THREAD} \)

Threshold: Investigate if -
Cost is \( \geq .2 \)

Note that all applications will have some branch mispredicts - it is not the number of mispredicts that is the problem but the impact.
To do hand-tuning, you need to locate the branch causing the mispredicts. This can be difficult to track down due to the fact that this event will normally tag to the first instruction in the correct path that the branch takes.
Machine Clears

- **Why:** Machine clears cause the pipeline to be flushed and the store buffers emptied, resulting in a significant latency penalty.
- **How:** General Exploration Profile, Metric: *Machine Clears*
- **Now What:**
  - If this metric is highlighted for your hotspot try to determine the cause using the specific events:
  - If MACHINE_CLEARS.MEMORY_ORDERING is significant, investigate at the sourcecode level. This could be caused by 4K aliasing conflicts or contention on a lock (both previous issues).
  - If MACHINE_CLEARS.SMC is significant, the clears are being caused by self-modifying code, which should be avoided.

Formula:

Machine Clear cost: \[
\frac{(MACHINE_CLEARS.MEMORY_ORDERING + MACHINE_CLEARS.SMC + MACHINE_CLEARS.MASKMOV) \times 100}{CPU_CLK_UNHALTED.THREAD}
\]

Threshold: Investigate if -
Cost is ≥ .02

Machine clears are generally caused by either contention on a lock, or failed memory disambiguation from 4k aliasing (both earlier issues). The other potential cause is self-modifying code (SMC).
Tuning for the Retiring Category

Retirement is:
• The completion of a micro-op's execution
• If the micro-op is the last micro-op for an instruction, it is also the completion of an instruction’s execution
• When results of an instruction’s execution are committed to the architectural state (cache, memory, etc)
In general, having as many pipeline slots retiring per cycle as possible is the goal. Besides algorithmic improvements like parallelism, there are two potential areas to investigate for the retiring category. The first is whether vectorization can be applied to make the instructions that are retiring even more efficient. See Code Study 1 – slide 22 – for more on this. The second is whether microcode assists can be eliminated from the instruction stream. See next 2 slides.
Retiring Hierarchical Breakdown in Amplifier XE

Expand Retiring to see the percentage of the Retiring slots classified as "General Retirement", which is the best case, vs "Microcode Sequencer", where the micro-ops retired were generated from the microcode sequencer (see next slide).
**Microcode Assists**

- **Why:** Assists from the microcode sequencer can have long latency penalties.
- **How:** General Exploration Profile, Metric: *Microcode Sequencer*
- **What Now:**
  - If this metric is highlighted for your hotspot, re-sample using the additional assist events to determine the cause.
  - If FP_ASSISTS_ANY / INST_RETIRED_ANY is significant, check for denormals. To fix enable FTZ and/or DAZ if using SSE/AVX instructions or scale your results up or down depending on the problem.
  - If (OTHER_ASSISTS.AVX_TO_SSE_NP*75) / (CPU_CLK_UNHALTED.THREAD) or (OTHER_ASSISTS.SSE_TO_AVX_NP*75) / (CPU_CLK_UNHALTED.THREAD) is greater than .1, reduce transitions between SSE and AVX code. See [http://software.intel.com/en-us/articles/avoiding-avx-sse-transition-penalties](http://software.intel.com/en-us/articles/avoiding-avx-sse-transition-penalties)

**Formula:**

Assist % = IDQ.MS_CYCLES / CPU_CLK_UNHALTED.THREAD

**Threshold:** Investigate if –

Assist Cost ≥ .05

There are many instructions that can cause assists when there is no performance problem. If you see MS_CYCLES it doesn’t necessarily mean there is an issue, but whenever you do see a significant amount of MS_CYCLES, check the other metrics to see if it’s one of the problems we mention.
The “Software on Hardware” Tuning Process

For each Hotspot

– Determine efficiency

  > If inefficient:
  • Determine primary bottleneck
  • Identify architectural reason for inefficiency
  • Optimize the issue

Repeat

Repeat until there are no significant hotspots or Retiring pipeline slots meet expectations
Good Luck!
For more information:

VTune Amplifier XE Videos, Forums, and Resources:  

Intel® 64 and IA-32 Architecture Software Developer’s Manuals:  

VTune Amplifier XE Tuning Guides for Other microarchitectures:  

For optimization of the integrated graphics controller:  
www.intel.com/software/gpa