Making the Most of Intel® Transactional Synchronisation Extensions

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Software and Services Group, Intel
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Notice revision #20110804
Agenda

• Intel® Transactional Synchronization Extensions (Intel® TSX)
• Enabling Intel TSX
• Intel TSX Optimization Workflow
• Monitoring and Profiling Intel TSX
• Root Causing Transaction Aborts
• Intel TSX Tuning Tips and Tricks
• Performance results
• Conclusion
Optimistic Non-blocking execution

Serialize execution only when necessary

Picture idea from Dave Boutcher
Transactional lock elision

Expose Concurrency & Eliminate Unnecessary Overhead
Intel® Transactional Synchronization Extensions

Two extensions of instruction set
• Hardware Lock Elision (HLE) – elision hints for LOCK instructions
• Explicit „Restricted Transactional Memory (RTM) instructions

Usages:
• Lock libraries to implement elided mutexes/rwlocks (HLE/RTM)
• Acceleration of transactional memory programming model
  – gcc 4.8: __transaction_atomic { c = a –b; }
RTM and HLE Hardware Implementation (Haswell, Broadwell, Skylake)

Buffering memory writes

• Hardware uses L1 cache to buffer transactional writes
  – Writes not visible to other threads until after commit
  – Eviction of transactionally written line causes abort
• Buffering at cache line granularity

Sufficient buffering for typical critical sections

• Cache associativity can occasionally be a limit
• Software (library) always provides fallback path in case of aborts

Hardware Manages All Transactional Writes
RTM and HLE Hardware Implementation (Haswell, Broadwell, Skylake)

Read and write addresses for conflict checking
• Tracked at cache line granularity using physical address
• L1 cache tracks addresses written to in transactional region
• L1 cache tracks addresses read from in transactional region
  – Additional implementation-specific probabilistic second level structure
  – Cache may evict address without loss of tracking

Data conflicts
• Detected at cache line granularity
• Detected using cache coherence protocol (R/W snoops)
• Occurs if at least one request is doing a write (strong isolation)
• Abort when conflicting access detected (“eager” protocol)

Hardware Automatically Detects Conflicting Accesses
RTM and HLE Hardware Implementation (Haswell, Broadwell, Skylake)

Transactional abort
- Occurs when abort condition is detected
- Hardware discards all transactional updates

Transactional commit
- Hardware makes transactional updates visible instantaneously
- No cross-thread/core/socket coordination required

Agenda

• Intel TSX - Introduction
• Enabling Intel TSX
• Intel TSX Optimization Workflow
• Monitoring and Profiling Intel TSX
• Root Causing Transaction Aborts
• Intel TSX Tuning Tips and Tricks
• Conclusion
## Comparison to Fine-Grained Locking or Lock-Free

<table>
<thead>
<tr>
<th></th>
<th>Coarse grained lock elision</th>
<th>Fine-grained locking or lock-free</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development complexity</td>
<td>low</td>
<td>high (race conditions, dead-locks, limited data width of atomic instructions)</td>
</tr>
<tr>
<td>Maintainbility</td>
<td>good (locking model well understood)</td>
<td>poor (experts required)</td>
</tr>
<tr>
<td>Overhead</td>
<td>low (only single Tx start/commit)</td>
<td>high (frequent long-latency atomic instructions)</td>
</tr>
<tr>
<td>Scalability</td>
<td>high</td>
<td>high</td>
</tr>
</tbody>
</table>

**Coarse grained lock elision: Scalable performance at coarse-grained development effort**
Enabling TSX using a TSX Lock Library

Intel® TBB 4.2 features *speculative_spin_mutex*

- HLE-based implementation of a speculative lock

RTM-based *speculative_spin_rwlock_mutex*

- Allows both concurrent speculative reads and concurrent writes
- Allows non-speculative readers to proceed together with speculations


Enabling TSX using a TSX Lock Library

Intel OpenMP (since Composer XE 2013 SP1)*

- export KMP_LOCK_KIND=adaptive to enable RTM adaptive elision for all omp_lock_t


- OpenMP 4.5 standard introduces (TSX) speculative hints
Enabling TSX using a TSX Lock Library

GLIBC PThreads 2.18

• configure with --enable-lock-elision=yes
  • SUSE SLES SP12 enables it by default
  • Other distros

• mutexes with PTHREAD_MUTEX_DEFAULT type are adaptively elided (RTM-based)

• PThreads 2.20: rwlocks can be elided too
Enabling TSX in Java (JDK8u20 onwards)

-XX:+UseRTMLocking option on the Java command line

- JVM will automatically use RTM instructions for synchronized statements and methods
- Adaptive lock elision (disabled/re-enabled based on commit statistics)

Additional tunings:

https://docs.oracle.com/javase/8/docs/technotes/tools/enhancements-8.html

https://bugs.openjdk.java.net/browse/JDK-8054376

https://bugs.openjdk.java.net/browse/JDK-8031320

Other lock libraries with TSX support

• Concurrency kit: spinlock elision with ck_elide wrappers
• Data plane development kit: "_tm" suffix to elide
  • Spin locks
  • Read-Write locks
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When to optimize with TSX (lock elision)

Contention on lock but small contention on data protected
- Different cache lines modified (read-read is not a contention)

Not too large
- data must fit into Tx buffer
- not too long: timer/interrupts abort

Not too small
- Min 100s of cycles, avoid tight transactions (HSW client)

Don't do TSX-unfriendly operations that always abort
Strategies to apply Intel TSX

**Elide all locks** -> analyze aborts -> optimize critical sections or disable elision for bad locks

**OR**

**Find good elision candidates**

- **Spin locks**: Many cycles in lock functions
  - Use VTune hotspot analysis or Linux „perf record cycles“
- „Sleeping“ locks: wait&spin time from Locks&Waits VTune analysis
The Workflow

1. Enable lock elision for (all/some) locks

2. Monitor TSX execution:
   - Too few cycles in transaction: check if right locks are elided: VTune locks&waits and mem_uops_retired.lock_loads PEBS sampling. Goto 1.
   - Build abort reason distribution

3. Find sources of aborts (IP -> source code)
   - Synchronous aborts (unfriendly instructions, page fault, etc): use a TSX profiler
   - Asynchronous aborts (conflicts, tx buffer overflow): only with a TSX emulator

4. Fix the aborts or disable elision. Goto 2
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Monitoring Intel TSX Execution (transactional/aborted cycles)

```bash
# perf stat -T ./program
```

Performance counter stats for './program':

- 62.890098 task-clock
- 77874071 instructions
- 108086139 cycles
- 68002201 raw 0x10000003c
- 67779742 raw 0x30000003c
- 15050 raw 0x1c9
- 0 raw 0x1c8

0.040780936 seconds time elapsed

```bash
#.pcm-tsx.x ./program
```

Intel(r) Performance Counter Monitor: Intel(r) Transactional Synchronization Extensions Monitoring Utility

Executing "./program" command:

Time elapsed: 42 ms

<table>
<thead>
<tr>
<th>Core</th>
<th>IPC</th>
<th>Instructions</th>
<th>Cycles</th>
<th>Transactional Cycles</th>
<th>Aborted Cycles</th>
<th>#RTM</th>
<th>#HLE</th>
<th>Cycles/Transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.58</td>
<td>47 M</td>
<td>81 M</td>
<td>33 M (40.81%)</td>
<td>127 K (0.16%)</td>
<td>7239</td>
<td>0</td>
<td>4583</td>
</tr>
<tr>
<td>1</td>
<td>1.13</td>
<td>3278 K</td>
<td>2905 K</td>
<td>0 (0.00%)</td>
<td>0 (0.00%)</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>0.84</td>
<td>3831 K</td>
<td>4566 K</td>
<td>2659 K (58.24%)</td>
<td>1460 (0.03%)</td>
<td>576</td>
<td>0</td>
<td>4617</td>
</tr>
<tr>
<td>3</td>
<td>0.74</td>
<td>33 M</td>
<td>45 M</td>
<td>32 M (70.23%)</td>
<td>85 K (0.19%)</td>
<td>7233</td>
<td>0</td>
<td>4446</td>
</tr>
<tr>
<td>*</td>
<td>0.66</td>
<td>88 M</td>
<td>134 M</td>
<td>68 M (50.56%)</td>
<td>214 K (0.16%)</td>
<td>15 K</td>
<td>0</td>
<td>4519</td>
</tr>
</tbody>
</table>

Perf tool from linux kernel 3.13+

Windows/any Linux/FreeBSD/OSX: Intel PCM-TSX tool
Success Metrics in Intel® VTune™ Amplifier XE

Choose Analysis Type

- Algorithm Analysis
  - Basic Hotspots
  - Advanced Hotspots
- Concurrency
- Locks and Waits

Microarchitecture Analysis
- General Exploration
- Bandwidth
- CPU Specific Analysis
  - Intel Core 2 Processor Ar
  - Nehalem / Westmere An
- Sandy Bridge Analysis
- Haswell Analysis
  - TSX Exploration
  - TSX Hotspots

TSX Exploration - Haswell

Analyze Intel Transactional Synchronization Extensions (Intel TSX) usage. This analysis type is based on the hardware event-based sampling collection. Press F1 for more details.

- Analyze user tasks

Select a step for analyzing TSX behavior. Start with measuring transactional success and then, if the aborts rate is high, analyze for aborts.

- 1. Transactional success
- 2. Aborts

Details

Events configured for CPU:

NOTE: For analysis purposes, Intel VTune Amplifier XE 2015 may adjust the Sample After values in the table below by a multiplier. The multiplier depends on the value of the

<table>
<thead>
<tr>
<th>Event Name</th>
<th>Sample After</th>
<th>Event Description</th>
</tr>
</thead>
</table>

Elapsed Time: 7.315s

- Clockticks: 420,000,638,400
- Transactional Cycles: 32,200,048,944
- Abort Cycles: 10,400,015,808
- Abort Cycles (%): 32.298
- Paused Time: 0s
Hardware events for abort (reason) statistics
### Intel TSX Perfmon Events (*why transactions aborted?*) (I)

<table>
<thead>
<tr>
<th>Event name</th>
<th>Event code</th>
<th>Event Unit mask</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTM/HLE_RETIRED.START</td>
<td>0xC9/0xC8</td>
<td>0x01</td>
<td>Number of times an RTM execution started.</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.COMMIT</td>
<td>0xC9/0xC8</td>
<td>0x02</td>
<td>Number of times an RTM execution successfully committed</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED</td>
<td>0xC9/0xC8</td>
<td>0x04</td>
<td>Number of times an RTM execution aborted due to any reasons (multiple categories may count as one)</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED_MISC1</td>
<td>0xC9/0xC8</td>
<td>0x08</td>
<td>Number of times an RTM execution aborted due to various memory events (conflict, overflow)</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED_MISC2</td>
<td>0xC9/0xC8</td>
<td>0x10</td>
<td>Number of times an RTM execution aborted due to uncommon conditions (watchdog, etc)</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED_MISC3</td>
<td>0xC9/0xC8</td>
<td>0x20</td>
<td>Number of times an RTM execution aborted due to RTM-unfriendly instructions</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED_MISC4</td>
<td>0xC9/0xC8</td>
<td>0x40</td>
<td>Number of times an RTM execution aborted due to incompatible memory type (MMIO, page fault)</td>
</tr>
<tr>
<td>RTM/HLE_RETIRED.ABORTED_MISC5</td>
<td>0xC9/0xC8</td>
<td>0x80</td>
<td>Number of times an RTM execution aborted due to none of the previous 4 categories (e.g. interrupt)</td>
</tr>
</tbody>
</table>
Intel TSX Perfmon Events *(why transactions aborted?)* (II)

<table>
<thead>
<tr>
<th>Event name</th>
<th>Event code</th>
<th>Event Unit mask</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_MEM.ABORT_CONFLICT</td>
<td>0x54</td>
<td>0x01</td>
<td>Number of times a transactional abort was signaled due to a data conflict on a transactionally accessed address</td>
</tr>
<tr>
<td>TX_MEM.ABORT_CAPACITY_WRITE</td>
<td>0x54</td>
<td>0x02</td>
<td>Number of times a transactional abort was signaled due to limited resources for transactional stores</td>
</tr>
<tr>
<td>TX_MEM.ABORT_HLE_STORE_TO_ELIDED_LOCK</td>
<td>0x54</td>
<td>0x04</td>
<td>Number of times a HLE transactional region aborted due to a non XRELEASE prefixed instruction writing to an elided lock in the elision buffer</td>
</tr>
<tr>
<td>TX_MEM.ABORT_HLE_ELISION_BUFFER_NOT_EMPTY</td>
<td>0x54</td>
<td>0x08</td>
<td>Number of times an HLE transactional execution aborted due to NoAllocatedElisionBuffer being nonzero.</td>
</tr>
<tr>
<td>TX_MEM.ABORT_HLE_ELISION_BUFFER_MISMATCH</td>
<td>0x54</td>
<td>0x10</td>
<td>Number of times an HLE transactional execution aborted due to XRELEASE lock not satisfying the address and value requirements in the elision buffer.</td>
</tr>
<tr>
<td>TX_MEM.ABORT_HLE_ELISION_BUFFER_UNSUPPORTED_D_ALIGNMENT</td>
<td>0x54</td>
<td>0x20</td>
<td>Number of times an HLE transactional execution aborted due to an unsupported read alignment from the elision buffer.</td>
</tr>
<tr>
<td>TX_MEM.ABORT_HLE_ELISION_BUFFER_FULL</td>
<td>0x54</td>
<td>0x40</td>
<td>Number of times HLE lock could not be elided due to Elision Buffer Available being zero.</td>
</tr>
</tbody>
</table>

**ABORT_CAPACITY** = RTM/HLE_RETIRED.ABORTED_MISC1 - TX_MEM.ABORT_CONFLICT
# Intel TSX Perfmon Events *(why transactions aborted?)* (III)

<table>
<thead>
<tr>
<th>Event name</th>
<th>Event code</th>
<th>Event Unit mask</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_EXEC.MISC1</td>
<td>0x5D</td>
<td>0x01</td>
<td>Counts the number of times a class of instructions that may cause a transactional abort was executed. Since this is the count of execution it may not always cause a transactional abort.</td>
</tr>
<tr>
<td>TX_EXEC.MISC2</td>
<td>0x5D</td>
<td>0x02</td>
<td>Counts the number of times a class of instructions that may cause a transactional abort was executed inside a transactional region</td>
</tr>
<tr>
<td>TX_EXEC.MISC3</td>
<td>0x5D</td>
<td>0x04</td>
<td>Counts the number of times an instruction execution caused the nest count supported to be exceeded</td>
</tr>
<tr>
<td>TX_EXEC.MISC4</td>
<td>0x5D</td>
<td>0x08</td>
<td>Counts the number of times an HLE XACQUIRE instruction was executed inside an RTM transactional region</td>
</tr>
</tbody>
</table>
Abort Reason Distribution

Use PMU counting mode with TSX events


**RTM:**

```bash
perf stat -e '{tx-abort-count,r8c9,r154,r20c9}' program
pcm-tsx program -e RTM RETIRED.ABORTED
                 -e RTM RETIRED.ABORTED_MISC1 -e TX_MEM.ABORT_CONFLICT
                 -e RTM RETIRED.ABORTED_MISC3
RTM -> HLE: tx -> e1; c9->c8 ;
```

#conflicts: TX_MEM.ABORT_CONFLICT
#Tx buf overflow: *_RETIRED.ABORTED_MISC1 - TX_MEM.ABORT_CONFLICT
#unfriendly instr: *_RETIRED.ABORTED_MISC3
#other: *_RETIRED.ABORTED - *_RETIRED.ABORTED_MISC1
                 - *_RETIRED.ABORTED_MISC3

Use additional TSX events to complete the picture
Linux perf stat with TSX events

```bash
perf stat -e r4c9 -e r8c9 -e r154 -e r20c9 ./matrix_tsx
```

Performance counter stats for './matrix_tsx':

- 14184836 raw 0x4c9
- 14171948 raw 0x8c9
- 14395057 raw 0x154
- 0 raw 0x20c9

9.410623956 seconds time elapsed

Here most aborts are conflicts: 0x4c9 ~= 0x154 (+ overcounting)
PCM-TSX with TSX events

pcm-tsx.x ./matrix_tsx -e RTM_RETIRED.ABORTED -e RTM_RETIRED.ABORTED_MISC1 -e TX_MEM.ABORT_CONFLICT -e RTM_RETIRED.ABORTED_MISC3

Intel(r) Performance Counter Monitor: Intel(r) Transactional Synchronization Extensions Monitoring Utility
Executing "./matrix_tsx" command:

Time elapsed: 9549 ms

**Event0: RTM_RETIRED.ABORTED** Number of times an RTM execution aborted due to any reasons (multiple categories may count as one) (raw 0x4c9)

**Event1: RTM_RETIRED.ABORTED_MISC1** Number of times an RTM execution aborted due to various memory events (raw 0x8c9)

**Event2: TX_MEM.ABORT_CONFLICT** Number of times a transactional abort was signalled due to a data conflict on a transactionally accessed address (raw 0x154)

**Event3: RTM_RETIRED.ABORTED_MISC3** Number of times an RTM execution aborted due to HLE-unfriendly instructions (raw 0x20c9)

<table>
<thead>
<tr>
<th>Core</th>
<th>Event0</th>
<th>Event1</th>
<th>Event2</th>
<th>Event3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8707 K</td>
<td>8701 K</td>
<td>8810 K</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>8247 K</td>
<td>8242 K</td>
<td>9231 K</td>
<td>0</td>
</tr>
</tbody>
</table>

* 16 M 16 M 18 M 0
Choose Analysis Type

TSX Exploration - Haswell

Analyze Intel Transactional Synchronization Extensions (Intel TSX) usage. This analysis type is based on the hardware event-based sampling collection. Press F1 for more details.

- Analyze user tasks

Select a step for analyzing TSX behavior. Start with measuring transactional success and then, if the aborts rate is high, analyze for aborts.

1. Transactional success
2. Aborts

Events configured for CPU:

事件 | Sample After | 事件描述
--- | --- | ---
HLE_RETIRED_ABORTED_PS | 10000 | 数字的倍数为HLE执行异常的个数（多个类别可能计数）。
RTM_RETIRED_ABORTED_PS | 10000 | 数字的倍数为RTM执行异常的个数（多个类别可能计数）。

Note that the result will be empty if #aborts < „Sample After“

Decrease the „Sample After“ if the workload has only a few aborts
TSX Exploration in Intel® VTune™ Amplifier XE

Instruction aborts are sync: can drill-down to exact instruction.

- Not precise
- Precise
Profiling Cycles Inside Transactions

Traditional profiling associate all cycles inside transactions to transaction begin instruction

Haswell adds hardware capability to show cycles correctly

Use profilers that support this new capability
Profiling Cycles Inside Transactions

Linux *perf* 3.13+:

```bash
perf record -e cycles:pp
```

Intel® VTune™ Amplifier XE:

<table>
<thead>
<tr>
<th>TSX Hotspots - Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analyze hotspots inside transactions for systems with the Intel Transactional Synchronization Extensions (Intel TSX) feature enabled. Press F1 for more details.</td>
</tr>
</tbody>
</table>

- **Collect stacks**
- **Analyze user tasks**

**Details**

Events configured for CPU:

NOTE: For analysis purposes, Intel VTune Amplifier XE 2015 may adjust the Sample After values in the table below by a multiplier. The multiplier depends on the platform.

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- Monitoring Intel TSX
- Root Causing Transaction Aborts
- Intel TSX Tuning Tips and Tricks
- Conclusion
Find Sources of Sync Aborts

Need a TSX enabled profiler

- Linux kernel 3.13 perf
- or Intel® Vtune™ Amplifier XE 2013 (TSX Exploration)

Collect abort sources with PEBS abort sampling:

RTM: `perf record -g --transaction --weight -e tx-aborts program`

HLE: `perf record -g --transaction --weight -e el-aborts program`

Show abort sources (weight=aborted cycles):

`perf report --sort symbol,dso,weight,transaction`
Find Sources of Async Aborts

Arrival of an abort „event“ is delayed/asynchronous

- tx buf overflow (loosing track of tx access) or conflict
- Perfmon/profiler can not tell killerIP

But: TSX emulation

- Big overhead, some aborts cannot be emulated (faults)
- But if many async aborts -> must show up in emulation too (reasoning statistically)

Intel Software Development Emulator


Intel SDE TSX Emulator

Options:  
- **-hsw** 
- **-hle_enabled 1** 
- **-rtm-mode full** 
- **-tsx_stats 1** 
- **-tsx_stats_call_stack 1**

- **Tx killer**  
  {instruction, IP, source code file and line, stack}
- Top abort sources by type
- Many other abort statistics
 Agenda

• Intel TSX - Introduction
• Enabling Intel TSX
• Intel TSX Optimization Workflow
• Monitoring and Profiling Intel TSX
• Root Causing Transaction Aborts
• Intel TSX Tuning Tips and Tricks
• Conclusion
Poor TSX lock Implementation

Anti-patterns:

• Retrying forever
• Not putting lock into read-set
• „Lemming effect“ = Persistent non-speculative execution
• Avoid unsupported lock elision patterns (same value on lock word restore, lock word size/address must match)
• Avoid unaligned accesses or partially overlapping accesses to the lock word
• Avoid writes to the lock word without XRELEASE instruction

Consult „TSX anti-patterns“ article or use a proven TSX lock from a standard library (TBB, PThreads, OpenMP, etc)
Reduce Generic Conflict Aborts

Avoid false-sharing

- Padding, data structure re-org helps

Avoid true-sharing

- Avoid global statistics and accounting: use sampling, per-thread stats, remove not critical stats, reduce windows of conflict (move bad accesses towards the tx end), use XTEST instruction

Sharing in memory allocators

- Use thread-friendly allocators (TBB, Google tcmalloc)

Silent stores: use conditional writes
Reduce Capacity/Overflow Aborts

- First time initialization: skip elision first time
- Check if particular cache sets are hot: use SDE emulator to log memory accesses inside transactions
- Change algorithm to touch less memory
- If cannot reduce the footprint: transit to fall-back early
Performance Studies
Performance: Java Hashtable/HashMap

- Hashtable

- HashMap

Put 0%  
Get 100%  
Remove 0%

Put 10%  
Get 80%  
Remove 10%
Performance: Java JSTAMP


![Graphs showing performance metrics for different applications: Sca2, Vacation, Genome, and Kmeans. The x-axis represents the number of threads, and the y-axis represents normalized execution time.]
Performance Evaluation of Intel R Transactional Synchronization Extensions for HPC

http://pcl.intel-research.net/publications/SC13-TSX.pdf

<table>
<thead>
<tr>
<th>Workload</th>
<th>Description</th>
<th>Threading</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>graphCluster</td>
<td>Performs min-cut graph clustering. Kernel 4 of SSCA2 [1].</td>
<td>OpenMP</td>
<td>locks</td>
</tr>
<tr>
<td>ua</td>
<td>Unstructured Adaptive (UA) from NAS Parallel Benchmarks suite [9]. Solves a set of heat equations on an adaptive mesh.</td>
<td>OpenMP</td>
<td>atomics</td>
</tr>
<tr>
<td>physicsSolver</td>
<td>Uses PSOR to solve a set of 3-D force constraints on groups of blocks.</td>
<td>PThread</td>
<td>locks</td>
</tr>
<tr>
<td>nufft</td>
<td>Non-uniform FFT. Baseline reported in [15].</td>
<td>OpenMP</td>
<td>locks</td>
</tr>
<tr>
<td>histogram</td>
<td>Parallel image histogram construction.</td>
<td>PThread</td>
<td>atomics</td>
</tr>
<tr>
<td>canneal</td>
<td>VLSI router from PARSEC [2]. Performs simulated annealing.</td>
<td>PThread</td>
<td>lock-free</td>
</tr>
</tbody>
</table>

![Graph](image)
TSX in Database studies

• HPCA 2014 Improving In-Memory Database Index Performance with Intel® Transactional Synchronization Extensions - Tomas Karnagel, Roman Dementiev, Ravi Rajwar, Konrad Lai, Thomas Legler, Benjamin Schlegel, Wolfgang Lehner (Intel, SAP AG and TU Dresden)

• EuroSys 2014 Using Restricted Transactional Memory to Build a Scalable In-Memory Database. - Zhaoguo Wang, Hao Qian, Jinyang Li, Haibo Chen (Fudan University, Shanghai Jiao Tong University, New York University)

• TDKE 2015 Scaling HTM-Supported Database Transactions to Many Cores - Viktor Leis, Alfons Kemper, Thomas Neumann (TU Munchen)
Intel TSX in a Commercial Database Product

Up to 2x performance boost in transactional processing when running SAP HANA database with TSX enabled

Baseline

- Intel Xeon processor E7 v2 family
- SAP HANA SPS 08

Configuration 1

- Intel Xeon processor E7 v2 family
- SAP HANA SPS 09

Configuration 2

- Intel Xeon processor E7 v3 family without Intel TSX enabled
- SAP HANA SPS 09

Configuration 3

- Intel Xeon processor E7 v3 family + Intel TSX enabled
- SAP HANA SPS 09

Improved transactions per minute (TPM):

- Baseline
  - Up to 1.8x more TPM

- Configuration 1
  - Up to 2.7x more TPM

- Configuration 3
  - Up to 6x more TPM

Figure 1. Upgrading to the Intel Xeon processor E7 v3 family and SAP HANA SPS 09 (S-OLTP stress test lab results) provides incremental performance gains.

Conclusion

• Intel TSX with lock elision is a simple technique to efficiently resolve locking and synchronization problems

• Tools for Intel TSX optimization are available

• Numerous studies show performance benefits

• Intel TSX tech resources + performance studies: www.intel.com/software/tsx
Transactional Lock Elision

- Thread 1:
  - Acquire
  - Critical section
  - Release

- Thread 2:
  - Acquire
  - Critical section
  - Release

- Hash Table:
  - Lock remains free throughout
  - Lock: Free
  - A
  - B

**No Serialization and No Communication if No Data Conflicts**
HLE/RTM Overview

HLE is a hint inserted in front of a LOCK operation to indicate a region is a candidate for lock elision
- XACQUIRE (0xF2) and XRELEASE (0xF3) prefixes
- Don’t actually acquire lock, but execute region speculatively
- Hardware buffers loads and stores, checkpoints registers
- Hardware attempts to commit atomically without locks
- If cannot do lock-free, restart and execute non-speculatively

RTM is three new instructions (XBEGIN, XEND, XABORT)
- Similar operation as HLE (except no locks, new ISA)
- If cannot commit atomically, go to handler indicated by XBEGIN
- Provides software additional functionality over HLE

XTEST is a new instruction to determine if in HLE or RTM
- Can be used inside both HLE and RTM
- Allows SW to query execution status of HLE and RTM
Enabling HLE in Custom locks

• Use intrinsics or direct machine code (compiler support needed) - see slides in backup for details

HLE Lock in Microsoft VC++

```cpp
#include <intrin.h> /* For _mm_pause() */
#include <imminitrin.h> /* For HLE intrinsics */
/* Lock initialized with 0 initially */
void acquire_lock(int *mutex) {
    while (_InterlockedCompareExchange_HLEAcquire(&mutex, 1, 0) != 0) {
        /* Wait for lock to become free again before retrying speculation */
        do {
            _mm_pause(); /* Abort speculation */
            /* prevent compiler instruction reordering and wait-loop skipping,
             * no additional fence instructions are generated on IA */
            _ReadWriteBarrier();
        } while (mutex == 1);
    }
}
void release_lock(int *mutex) {
    _Store_HLERelease (mutex, 0); // was mutex = 0; in non-HLE version
}
```
RTM Intrisics

gcc 4.8 (–mrtm flag), Microsoft Visual Studio 2012, Intel® C++ Compiler XE 13.0

_xbegin(): attempt transaction. Returns status
- _XBEGIN_STARTED (-1): in transaction
- Otherwise abort code with bits:

<table>
<thead>
<tr>
<th>_XABORT_EXPLICIT</th>
<th>Abort caused by _xabort(). _XABORT_CODE(status) contains the value passed to _xabort()</th>
</tr>
</thead>
<tbody>
<tr>
<td>_XABORT_RETRY</td>
<td>When this bit is set retrying the transaction has a chance to commit. If not set retrying will likely not succeed.</td>
</tr>
<tr>
<td>_XABORT_CONFLICT</td>
<td>Another thread / processor conflicted with a memory address that was part of this thread's transaction.</td>
</tr>
<tr>
<td>_XABORT_CAPACITY</td>
<td>The abort is related to a capacity overflow</td>
</tr>
<tr>
<td>_XABORT_DEBUG</td>
<td>The abort happened due to a debug trap</td>
</tr>
<tr>
<td>_XABORT_NESTED</td>
<td>The abort happened in a nested transaction</td>
</tr>
</tbody>
</table>

_xend(): commit transaction
_xtest(): true if in transaction
_xabort(constant): aborts current transaction
Enabling RTM with a Lock Wrapper (basic, no retries, etc)

```c
void elided_lock_wrapper(lock) {
    if (_xbegin() == _XBEGIN_STARTED) { /* Start transaction */
        if (lock is free) /* Check lock and put into read-set */
            return; /* Execute lock region in transaction */

        _xabort(0xff); /* Abort transaction as lock is busy */
    } /* Abort comes here */

    // abort handler: optionally analyze abort flags, retry with xbegin...
    take fallback lock
}

void elided_unlock_wrapper(lock) {
    if (lock is free)
        _xend(); /* Commit transaction */
    else
        unlock lock;
}
```

HLE in Linux (Intel® C++ Compiler and gcc)

**Inline asm:**

```c
#define XACQUIRE ".byte 0xf2; "
#define XRELEASE ".byte 0xf3; "
static inline int hle_acquire_xchg(int *lock, int val)
{
    asm volatile(XACQUIRE "xchg %0,%1":"+r" (val), "+m" (*lock) :: "memory");
    return val;
}
static void hle_release_store(int *lock, int val)
{
    asm volatile(XRELEASE "mov %0,%1":"r" (val), "+m" (*lock) :: "memory");
}
```
HLE Intrisics in gcc 4.8

Caution: needs –O2 or higher opt (compiler bug)

__ATOMIC_HLE_ACQUIRE and __ATOMIC_HLE_RELEASE flags for

__atomic_compare_exchange_n,

__atomic_store,

__atomic_clear, etc

intrisics
Other Compilers with HLE support

C++11 `<atomic>` in gcc 4.8: extended memory models: __memory_order_hle_acquire and __memory_order_hle_release
• i.e. for atomic_flag::test_and_test(..), clear(..), etc

Windows: Intel and Microsoft compilers
• `_InterlockedCompareExchange{,64,Pointer}_HLE{Acquire, Release}`
• `_InterlockedExchangeAdd_HLE{Acquire, Release}`
• `_Store{,64,Pointer}_HLERelease`
Reduce Conflict Aborts in Lock Elision
„lemming effect“ (persistent non-spec execution)

Lock word is in the read-set

- Lock Elision specific (both with HLE and RTM)
- Non-spec lock acquisition -> conflict on lock word
  - Avoid „lemming effect“ (persistent non-spec execution)
- Solution: wait outside transaction (non-HLE path or abort handler) for fall-back lock to be free and only then respeculate/retry

See also http://software.intel.com/en-us/articles/tsx-anti-patterns-in-lock-elision-code
(Single-Threaded) Transaction Overheads

The overhead is amortized in larger critical sections but will be exposed in very small critical sections.

One simple approach to reduce perceived overhead is to perform an access to the transactional cache lines early in the critical section.
Contention (conflicts) in SDE (I)

sde-tsx-stats.txt:
# COUNTERS OF TSX ABORTS PER ABORT REASON
#---------------------------------------------------------------
# REASON                         RTM ABORTS   HLE ABORTS
ABORT_CONTENTION                     6559            0

Transaction killers:

# TOP 10 CONTENTION ABORTS
#---------------------------------------------------------------
#     IP     COUNT   INSTRUCTION DISASSEMBLY
0x000000000000400ddf     3993   mov eax, dword ptr [rax+0x10]
0x000000000000400ec2     2519   mov dword ptr [rax+0x10], 0x1
0x0000000000004008b2          31   mov eax, dword ptr [rax+0x4]
0x00000000000040104e            7   mov eax, dword ptr [rax+0x10]
0x000000000000400ed0            3   mov dword ptr [rax+0x8], edx
0x000000000000401117            3   mov dword ptr [rax+0x10], 0x1
0x000000000000400e24            1   mov eax, dword ptr [rax+0x10]
0x000000000000400eeb            1   mov dword ptr [rax+0xc], edx
0x000000000000400fbb            1   mov eax, dword ptr [rax+0x10]
Contestion (conflicts) in SDE (II)

# STACK INFORMATION FOR CONTENTION ABORT KILLER IP: 0x0000000000400ddf

<table>
<thead>
<tr>
<th>#</th>
<th>IP</th>
<th>FUNCTION NAME</th>
<th>FILE NAME</th>
<th>LINE</th>
<th>COLUMN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00007fe4cf526520</td>
<td>start_thread</td>
<td>/root/FP/double/matrix_tsx.c</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x00000000004015d6</td>
<td>worker</td>
<td>/root/FP/double/matrix_tsx.c</td>
<td>56</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x0000000000400d78</td>
<td>call_tsx_fasttrack_read</td>
<td>/root/FP/double/fasttrack_tsx.h</td>
<td>148</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x0000000000400ddf</td>
<td>call_tsx_fasttrack_read</td>
<td>/root/FP/double/fasttrack_tsx.h</td>
<td>159</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

# STACK INFORMATION FOR CONTENTION ABORT KILLER IP: 0x0000000000400ec2

<table>
<thead>
<tr>
<th>#</th>
<th>IP</th>
<th>FUNCTION NAME</th>
<th>FILE NAME</th>
<th>LINE</th>
<th>COLUMN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00007fe4cf526520</td>
<td>start_thread</td>
<td>/root/FP/double/matrix_tsx.c</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x00000000004015d6</td>
<td>worker</td>
<td>/root/FP/double/matrix_tsx.c</td>
<td>56</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x00000000004013fd</td>
<td>mm</td>
<td>/root/FP/double/matrix_tsx.c</td>
<td>30</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x0000000000400d78</td>
<td>call_tsx_fasttrack_read</td>
<td>/root/FP/double/fasttrack_tsx.h</td>
<td>148</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x0000000000400ef0</td>
<td>call_tsx_fasttrack_read</td>
<td>/root/FP/double/fasttrack_tsx.h</td>
<td>188</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0x0000000000400ec2</td>
<td>call_tsx_fasttrack_read</td>
<td>/root/FP/double/fasttrack_tsx.h</td>
<td>182</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

# LIST OF TSX CONTENTION ABORT EVENTS

<table>
<thead>
<tr>
<th>#</th>
<th>TID</th>
<th>TRANSACTION IP</th>
<th>KILLER TID</th>
<th>KILLER IP</th>
<th>KILLER DATA ADDRESS</th>
<th>INSIDE TSX</th>
<th>TSX TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0x000000000040138e</td>
<td>2 0x0000000000400ec2</td>
<td>0x00000000006067e0</td>
<td>YES</td>
<td>RTM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0x000000000040138e</td>
<td>1 0x00000000004008b2</td>
<td>0x00000000006066e4</td>
<td>YES</td>
<td>RTM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0x000000000040138e</td>
<td>2 0x000000000040fbb</td>
<td>0x0000000000608408</td>
<td>YES</td>
<td>RTM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0x000000000040138e</td>
<td>1 0x0000000000400ec2</td>
<td>0x00000000006065d8</td>
<td>YES</td>
<td>RTM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<------------------------------------------------------------------------------------------------------------------->
Instruction Specific Aborts

• Legacy X87 math (long double)/MMX -> use SSE/AVX math (compiler switch)
• X87 for function parameters -> inline
• SSE/XMM regs AVX instruction mix, VZEROUPPER -> avoid
• Avoid ring transitions: SYSENTER, SYSCALL, SYSEXIT, SYSRET
• Segment, control, debug regs (kernel) -> move outside Tx
CPU Faults and Traps

• Instruction page faults, segm faults, divide errors, breakpoint, other exceptions are suppressed -> reexecute exactly the same path without elision to resolve the fault and/or debug the error

Higher abort rate on program start up:

• Data page faults (memory init, program startup) -> skip elision for first time -> ok then

• Core sets Accessed and Dirty Bits in page table: skip elision for first time -> ok then
Background (Noise-level) Aborts

Not a problem – should be just noise level

- NMI, SMI, INTR, IPI, PMI, timer ticks, etc
- L3 cache inclusion aborts
- Rare uarch conditions
- Handling corner cases with ucode (rare)
Still Observing Aborts?

- One-time or temporal aborts: transition to fall-back early (XABORT or lock acquire commit), skip elision for some time (once)

- Disable TSX elision for selected lock

Aborts/retries may be better than taking lock

- TSX with low commit/abort ratio may still outperform locks (better to retry than waste time in waiting for the lock)

- Taking lock is very expensive on servers (all 100s threads serialize): Tx retrying without serializing other threads is cheaper
Further Reading

• Intel TSX tech resources + performance studies: www.intel.com/software/tsx