Control Flow Enforcement Technology (CET)

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Agenda

- Introduction
- Motivation
- Technology overview
  - Shadow Stack
  - Endbranch
- LLVM Compiler enabling
- Summary
Modern CPU enhancements prevent code injection: Non-executable stack and non-writeable code pages

However: IA allows instruction decoding to start from any byte, providing attackers with a different set of instructions than intended by the programmer

Attackers scan the code for meaningful snippets (gadgets) and chain them together through:
- ROP – “Return” oriented programming
- JOP – “Jump” oriented programming
- COP – “Call” oriented programming
Intel’s Control-flow Enforcement Technology - CET

- **Goals**
  - SW friendly ISA to protect from ROP/COP/JOP
  - Comprehensive solution with minimal impact to application developers
  - Broad enabling via OS, Dev Tools and Runtime
  - Acceptable performance and impact on energy usages

- **Architecture**
  - Two mechanisms to enhance protection against unintended changes to execution flow
  - ROP: SHADOW-STACK for protecting return addresses
  - JOP/COP: ENDBRANCH instruction for marking legal target addresses of indirect jumps and calls
  - Each mechanism can be enabled separately per privilege level
Shadow Stack Operation

- **Call**
  - pushes return address on both stacks
- **No parameters passing on shadow stack**

- **Return**
  - pops return address from both stacks
  - Controlflow Protection (#CP) exception in case the two return addresses don’t match

**Stack usage on near CALL**

- **ESP after call**
  - ESP after ret
  - Stack
    - Return EIPn-1
    - Param 1
    - Param 2
    - Return EIPn
- **ESP after ret**
  - SSP after call

**SHADOW STACK**

- Setup by OS/VMM
- Protected by new memory access control
- Different shadow stacks for each privilege level

**Keeps stack ABI intact – no changes to data stack layout**
Managing the Shadow Stack

- OS/VMM sets up the Shadow stack for the application
- Some usages require to manage the Shadow Stack pointer
  - Stack unwinding
  - User mode thread switching
- New instructions help manage shadow stack securely:
  - RDSSP + INCSSP – To set checkpoint and unwind stack
  - SAVEPREVSSP/RSTORSSP – save/restore shadow stack pointer for user mode thread switching
- Full list in spec

Minimal changes to securely support common software constructs
New Instruction to mark legal targets of indirect jumps

Added by the compiler

Decodes as “NOP” on legacy processors

An indirect jump to a target not marked by ENDBR signals an exception
Separate state machines for user and for supervisor mode

Special no-track prefix for protected jumps to reduce ENDBRANCH footprint

Special treatment for debugging (INT3 opcode “CC”)
Compatibility with legacy libraries

- Legacy libraries don’t have ENDBRANCH and could crash the application
- OS/VMM can set the legacy compatibility treatment bitmap for the context
  - If the bitmap indicates page has endbranch-enabled code, #CP exception is signaled
  - If the bitmap indicates page has legacy code, the violation is waived
- OS can choose between a one-time waiver and suspending endbranch violations until an ENDBR32/64 is detected
- Legacy compatibility treatment could potentially greatly impact performance, so users are encouraged to use recompiled libraries
COMPILER SUPPORT
ABI Changes

- Updated System V ABI with Intel CET extension

- Program loader Updates
  - Enables Shadow-Stack (SHSTK) if the executable and all shared objects are SHSTK enabled
  - Enables Indirect Branch Tracking (IBT) if the executable is IBT enabled and mark non-IBT enabled shared objects as legacy using an allocated bitmap

- The linker creates IBT-enabled PLT
Compiler CET Considerations

- Compilers minimize the use of ENDBR instruction in order to:
  - Avoid possible attacker landing pads
  - Reduce code size (consider huge switch cases)

- For guarded (range check) switch cases, ENDBR instructions are not added

- The compiler doesn’t always know which function will be called by indirect call

- Compiler provides ‘no_track’ attribute:
  - Function: To avoid ‘ENDBR’ at the beginning of a function
  - Function Pointer: To add ‘no_track’ prefix before an indirect call

- Compiler updates exceptions handling builtins to fix the shadow stack
  - For example: To fix shadow stack pointer after SetJmp/LongJmp
Compiler Status

- GCC/LLVM/ICC/MS compilers have started implementing CET support
- GCC team updates GNU libraries, loader and linker
- LLVM is currently in the stage of open-sourcing CET support
Summary

- Intel’s Control-Flow Enforcement Technology (CET) provides a comprehensive solution to enhance protection against ROP/JOP/COP attacks
  - SHADOW STACK: Enhanced protection against ROP attacks
  - ENDBRANCH: Enhanced protection against JOP/COP attacks
- Protects applications and supervisor code
- Minimal impact to existing SW and to application developers
- Spec is published, search for intel CET