Parallel Programming: Embracing a New Era of Highly Efficient and Productive Quantum Monte Carlo Simulations

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Code Modernization of QMCPACK

Optimization Techniques:
1. Stick to C++ and OpenMP 4.0 standards
2. Develop minapps.
3. Implement new containers in structure-of-arrays (SoA) data layout
4. Facilitate auto-vectorization by the compilers.
5. Computing data on the fly with the vectorized routines.
6. Expanding the use of single-precision calculations.

QMCPACK Introduction

An open-source US-DOE flagship many-body sub into quantum Monte Carlo (QMCPACK) code for computing the electronic structure of atoms, molecules, and solids.

http://qmcpack.org/

[Image of parallel efficiency of QMCPACK on US DOE facilities.]

Diffusion Monte Carlo Schemes

Ensemble changes according to
- Old configurations
- Random Waking
- Possible new configurations
- New configurations

Old configurations
- Diffusion
- Drill
- Branching

New configurations
- w=0.8
- w=1.6
- w=2.4
- w=3.0
- w=3.4


Data Structure Conversion – AoS to SoA

- Use full NxNp (with padding) array instead of using compact storage.
- Enables efficient vectorization with aligned computations.
- Delay update to the upper part of the matrix – only update lower part during OpenMP move.
- Compute on the fly instead of storing intermediate results.

Schematics for AA (symmetric) distance table management (a) before and (b) after the optimizations. vi is a separate array to hold the temporary data for the i-th electron move. The column update in (b) is later removed with the compute on the fly optimization.

Energy usage of NiO-32 benchmark on KNL.

Memory usage on KNL processor.

Strong scaling of NO-64 benchmark on Trinity at LANL (KNL) and Serrano at SNL (BDW) systems. The performance is normalized by a reference throughput using 64 BDW sockets. Slopes of the ideal-scaling lines are provided in parentheses.

Systems
- Second generation Intel® Xeon® Phi™ processor 7250P-DA (KNL) dual socket Intel® Xeon® E5-2690v4 (BDW)
- Cluster (1) at Los Alamos National Laboratory with KNL processors and Cray Aries Dragonfly interconnect (2) Serrano cluster at Sandia National Laboratories with dual-socket BDW processors and Intel® Ociex-Path interconnect
- Intel® Parallel Studio XE 2017 on Intel® platforms with the following compiler flags: -O3 -ipo -v -inline -march= intel64 -qopt-report=level1 -qopt-report=ml -openmp:static =v1, with simd=AVX,KNL=AVX512, default =AVX2
- Advanced high performance computing with Intel® Xeon®. Amplifier 2017 (Intel®) performance analysis with an engineering version of Amplifier 2017 (Intel®). Amplifier 2017 is an Intel® Xeon® 1770 processor with two 1750MHz cores and two 1820MHz cores. Amplifier 2017 was used on a single socket Intel® Xeon® 1770 processor. Amplifier 2017 is an Intel® parallel analysis tool that is semi-exhaustive in that it explores part of the option space. Amplifier 2017 provides a no-cost performance analysis tool that is easy to use and provide insights into the factors that influence performance. Amplifier 2017 is a part of the Intel Parallel Studio XE family of products. Amplifier 2017 provides a no-cost, easy-to-use, performance analysis tool that is available for Windows and Linux platforms. Amplifier 2017 is a part of the Intel Parallel Studio XE family of products. Amplifier 2017 provides a no-cost, easy-to-use, performance analysis tool that is available for Windows and Linux platforms.