ACCELERATING WORKLOADS USING THE ACCELERATION STACK FOR INTEL® XEON® CPU WITH FPGAS

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UNLEASH FPGA ACCELERATION

FPGA design development has traditionally required FPGA hardware expertise. The Acceleration Stack for Intel® Xeon® CPU with FPGAs enables application developers to accelerate their workloads with FPGAs easily, portably, and without deep FPGA knowledge.

The Acceleration Stack provides multiple benefits:
• Saves developer time to focus on their solution
• Enables code-reuse across Intel Xeon + FPGA products
• Establishes the world’s first common developer interface for Intel FPGA Data Center products
• Offers optimized and simplified hardware and software APIs provided by Intel
• Supports OpenCL™ and RTL development flows to provide flexibility

DEEP LEARNING

The Intel® Deep Learning Toolkit runs the AlexNet Image classification algorithm on the FPGA and sends the classification results to Xeon which runs a web service depicting images as they are classified and displays the classification scores.

GENOMICS – PAIR HMM

Intel FPGAs speed up pairHMM in the HaplotypeCaller function of the GATK variant calling tool, resulting in 20% overall speed up to Broad’s application pipeline.

ACCELERATION STACK FOR INTEL XEON® CPU WITH FPGAS

(with Open Programmable Acceleration Engine technology)

https://github.com/OPAE/opae-sdk

ACCELERATOR INTERFACE

• Accelerator developers are presented an open specification called CCI-P for PCIe communication
• CCI-P is available on all Intel Xeon® + FPGA products ensuring portability across present platforms and forward compatibility to future platforms with next-generation interfaces
• Private memory is accessed using the open Avalon Memory Mapped specification
• 40Gb/s network interface is accessible using the open Avalon Streaming specification

INTEL® PROGRAMMABLE ACCELERATION CARD WITH INTEL® ARRIA® 10 GX FPGA

• 1.15 million logic element FPGA
• PCIe Gen3x8
• 8GB DDR4 memory
• 40Gb/s capable QSFP+ interface
• On-board flash with runtime FPGA image & factory recovery image
• Board Management Controller, enabling remote management across PCIe sideband channels

CONCLUSION

• The Acceleration Stack for Intel Xeon® CPU with FPGAs removes traditional barriers enabling software and hardware developers to leverage FPGAs for workload acceleration.
• Learn more at https://www.altera.com/solutions/acceleration-hub/overview.html
• The Open Programmable Acceleration Engine enables faster development of accelerator functions and is upstreamed into Linux kernel (https://github.com/OPAE/opae-sdk)
• OPAE and the Acceleration Stack provide an open, forward compatible framework enabling developers to leverage their development investment over many technology generations significantly increasing ROI